

CS 152 Midterm 1

March 5, 2002

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Name _____SOLUTIONS_____

Show your work if you want partial credit!

Try all the problems, don't get stuck on one of them. Each one is worth 10 points.

1)_____

2)_____

3)_____

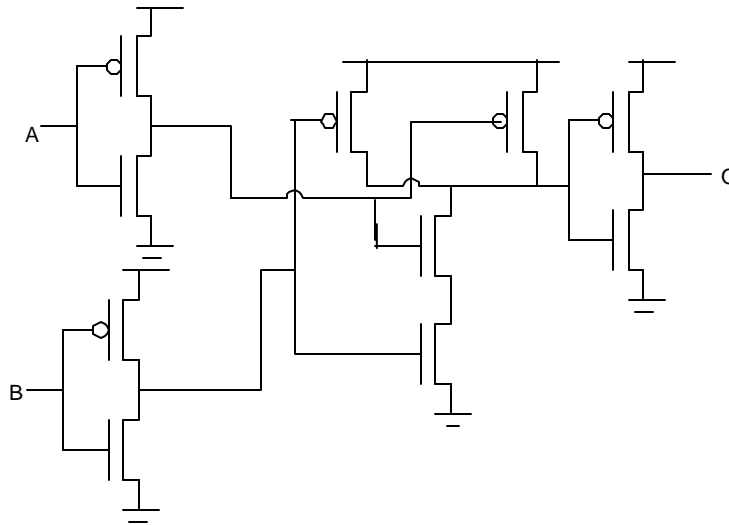
4)_____

5)_____

6)_____

7)_____

Problem 1)



a) What logic function of A & B to O does the above gate perform?

NOR

Assume the following:

- i) the only capacitance comes from the input gate of the transistors
- ii) that all the transistors have the same input (gate) capacitance, C_g
- iii) the NMOS “on” Resistance is R
- iv) the PMOS “on” resistance is $3R$.
- iv) only A is making a transition and B is low

b) What is the worst case condition for the internal delay (i.e. what direction is the transition at A) – justify your answer.

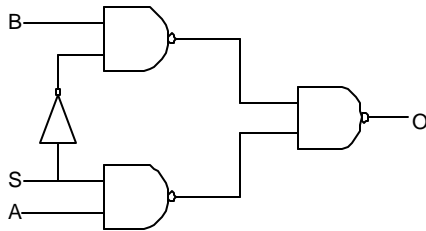
Inv. Nand

A High-to-Low $(3R)2C + (2R)2C = 10RC$

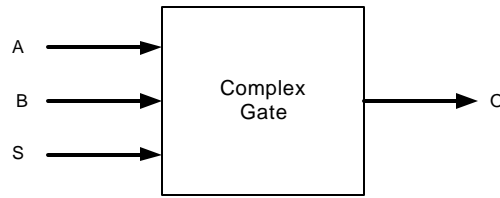
A Low-to-High $(R)2C + (3R)2C = 8RC$

Problem 2)

a)



b)



NAND: Input Capacitance: 50fF, $t_{pHL} : 0.5ns$, $t_{pLH} : 0.4ns$, $t_{pHLf} : 0.03ns/fF$, $t_{pLHf} : 0.02ns/fF$

INV: Input Capacitance: 20fF, $t_{pLH} : 0.3ns$, $t_{pHL} : 0.2ns$, $t_{pHLf} : 0.01ns/fF$, $t_{pLHf} : 0.005 ns/fF$

Figure a) is the internal logic for the complex gate of figure b). The problem is to calculate the necessary parameters to characterize its delay characteristics of the complex gate.

Give the following values for the complex gate:

C_{in} for S: **70fF**

C_{in} for A: **50fF**

C_{in} for B: **50fF**

The following three load dependent delays (low to high from A->O and high to low from S->O and high to low from B->O)

$t_{aolhf} : .02ns/fF$

$t_{sohlf} : .03ns/fF$

$t_{bohlf} : .03ns/fF$

Calculate the following internal delays (high-to-low at O from A->O, B->O and S->O).

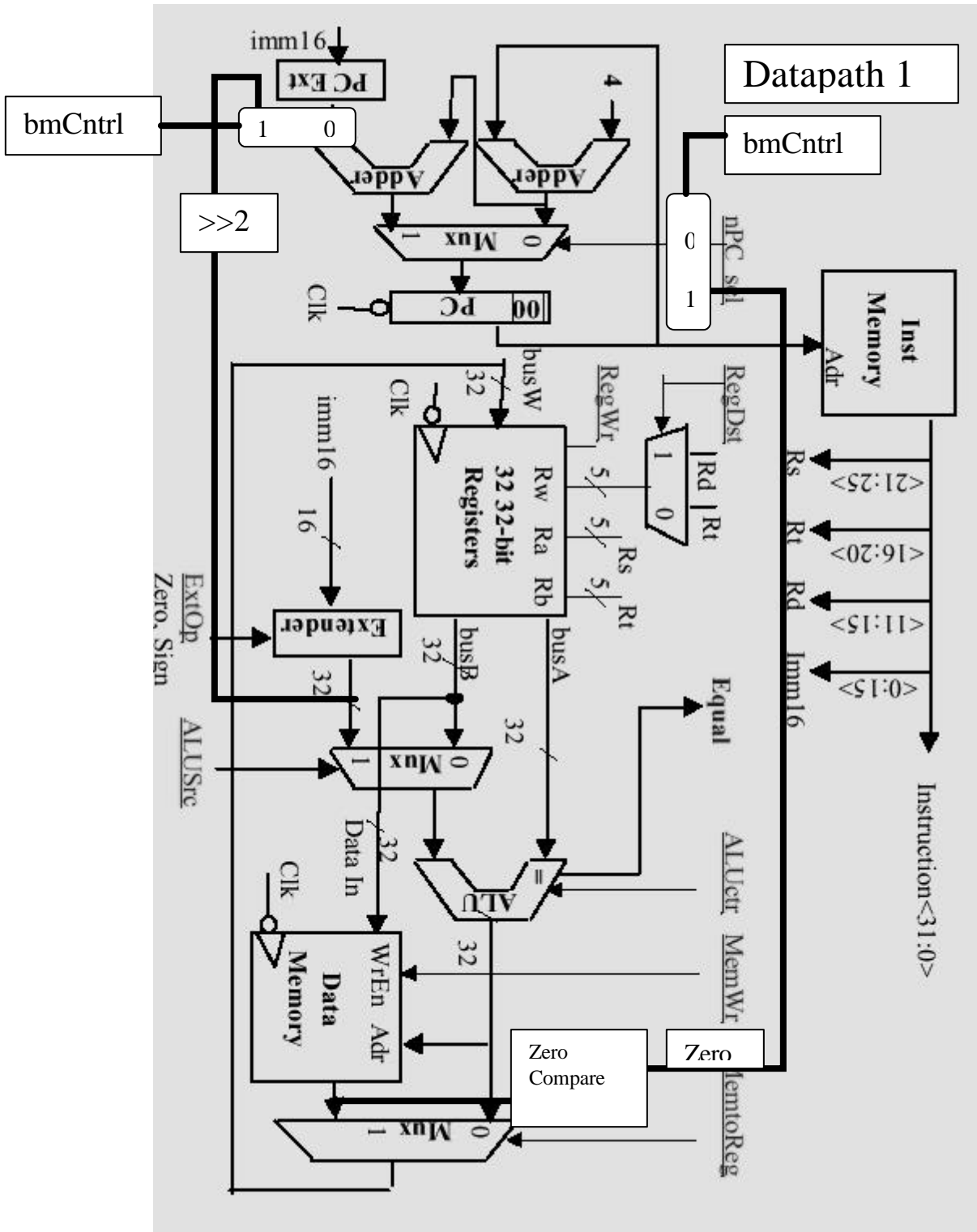
$t_{aohl} : 1.9ns$

$t_{bohl} : 1.9ns$

$t_{sohl} : 2.6ns$

A->O, B->O $.5ns + (.02)50 + .4ns$

S->O $.2ns + (.01)50 + .4 + (.02)50 + .5 = 2.6$



Problem 3

Fill in the following table for control signals for the following instructions for Datapath1 on the previous page.

ADDU $R[rd] \leftarrow R[rs] + R[rt];$

$PC \leftarrow PC + 4$

LOAD $R[rt] \leftarrow MEM[R[rs] + sign_ext(Imm16)];$

$PC \leftarrow PC + 4$

(a)

	RegDst	nPCsel	ExtOp	MemtoReg	ALUOp	MemWr	ALUSrc	RegWr
addu	1	0	X	0	Add	0	0	1
lw	0	0	sign	1	Add	0	1	1

ALUOp can be add, subtract, Or

MemWr and RegWr are high when writing

(b) Draw the critical path for addu on the datapath using a dashed line and describe it below (e.g. PC->Instr Mem->....)

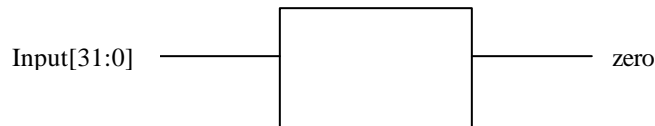
PC->InstrMem->Reg Access->MUX->ALU delay->MUX->Reg Setup

Problem 4)

Suppose we wish to add support for the new instruction, bmez: branch if memory equals zero, into Datapath 1. The format of the instruction is as follows,

bmez \$rt, \$rs, imm16

The instruction reads the value of memory in address (R[\$rs] + R[\$rt]), compares it to zero and if zero then branches to the zero extended immediate, otherwise it goes on to the next instruction. You can add logic gates and muxes, and the zero compare block below, and one new control signal, bmCntrl.



zero is high when the Input is zero.

a) Modify Datapath 1 to support this instruction and show its critical path. Also, describe below your modifications in words.

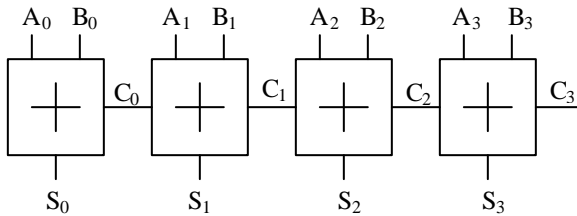
Add a zero compare block to the output of the memory, then mux the zero flag with nPCsel under control of bmCntrl.

To get the Zero extended immediate, we need to mux the output of the extend block to the input of the branch adder

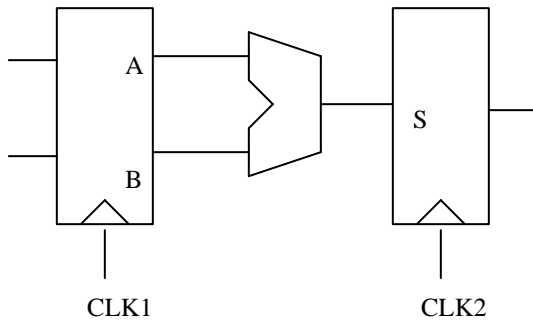
b) Give the value of the control lines for the new instruction

	RegDst	nPCsel	ExtOp	MemtoReg	ALUOp	MemWr	ALUSrc	RegWr	bmCntrl
bmez	X	X	zero	X	Add	0	0	0	1

Problem 5) We have a 4-bit carry ripple adder:



Now, suppose, we have the following setup:



The one-bit full adder blocks have the following delay properties:

$$A_i \rightarrow S_i = B_i \rightarrow S_i = 6\text{ns}, A_i \rightarrow C_i = B_i \rightarrow C_i = 3\text{ns}, C_{i-1} \rightarrow S_i = 3\text{ns}, C_{i-1} \rightarrow C_i = 2\text{ns}$$

The registers have the following properties: $t_{\text{clk-to-q}}=3\text{ns}$, $t_{\text{setup}} = 2\text{ns}$, $t_{\text{hold}}=1\text{ns}$

(a) What is the maximum clock frequency we can run this circuit at, assuming $\text{CLK1}=\text{CLK2}$ (no clock skew?)

$$\text{clk-to-Q} + A0 \rightarrow C0 \rightarrow C1 \rightarrow C2 \rightarrow S3 + \text{setup} < \text{Cycle time}$$

$$3 + 3 + 2 + 2 + 3 + 2 = 15 \text{ ns}$$

$$\text{Maximum clock rate} = 1/15\text{ns} = 66 \text{ MHz}$$

b) If there is a clock skew of 3 ns with CLK2 later from CLK1, what is the maximum clock frequency?

$$1/(15-3) = 83 \text{ MHz}$$

(b) What is the maximum worst case clock skew that this circuit can tolerate before there is a race condition?

$$\text{CLK-to-Q} + \text{Shortest Path} - t_{\text{hold}} > \text{Clock Skew}$$

$$3\text{ns} + 6\text{ns} - t_{\text{hold}} = 8\text{ns} > \text{Clock Skew}$$

(c) What direction is the skew for this worse case condition (i.e. is CLK1 before or after CLK2)? **CLK1 is before CLK2**

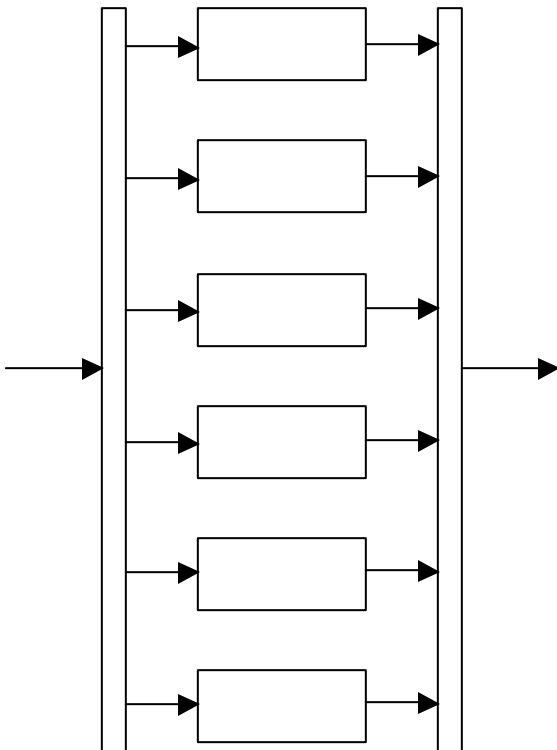
Problem 6)

Assume the dependence of the critical path delay on supply voltage of the adder and register circuit in problem 5 is given by $t_{\text{delay}} = 5\text{ns} (2.8/(V_{\text{dd}}-.5))$. Therefore the delay with a 3.3 volt supply is 5 ns. and the maximum clock rate is 200MHz and lets assume that our system requirement is just met by operation at this speed.

The problem is to reduce the power consumption as much as possible by reducing the supply to 1 volt and using parallelism to meet the throughput requirements in spite of the fact that the delays have increased.

Calculate the result for parallelism obtained by duplicating the hardware and operating in parallel. (Ignore the overhead in delay and power due to muxes and registers required for increasing the parallelism.)

a) Draw the new architecture showing the parallel units and any muxing required.



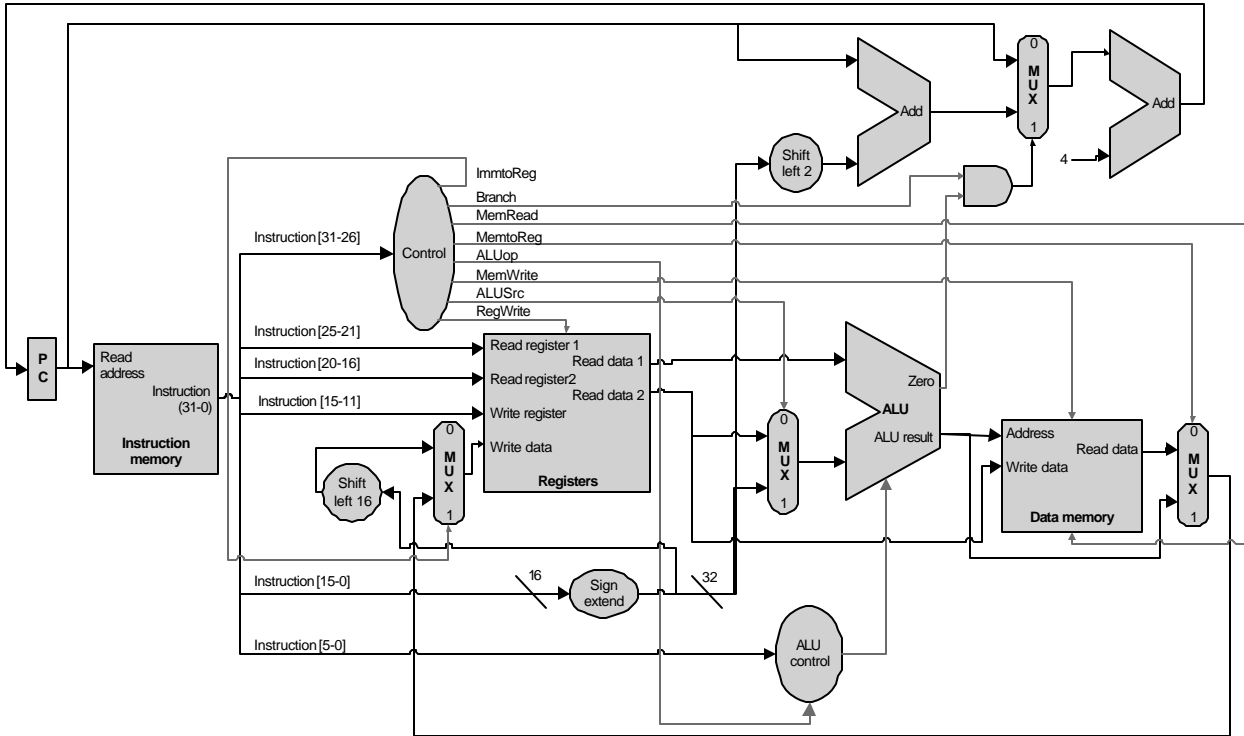
Delay at 1 volt is $= 5\text{ns} * 2.8/(1-.5) = 5*5.6$. This means we need at least 6 units to get the same throughput (since we can't do a fractional unit). With 6 units the clock rate can be 6 times slower for the same throughput or $200\text{MHz}/6 = 33\text{MHz}$

b) What is the new minimum Clock rate ? 33MHz :

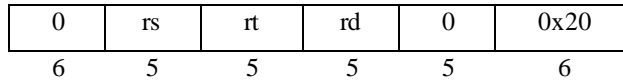
c) How much of a power reduction was obtained? $\frac{6C * 1^2 * (f/6)}{C*(3.3)^2 * f}$

Power= CV^2f

Problem 7) Some of the following instructions can *not* be carried out in the provided datapath. Explain why in the space after each instruction that can't be implemented.

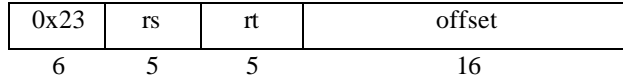


1) add rd, rs, rt



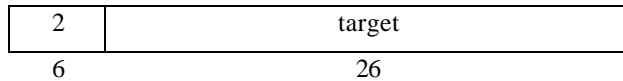
OK

2) lw rt, offset(rs)



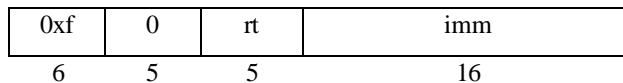
Can't provide Rt as an address to write to the Reg file (mux missing)

3) j target



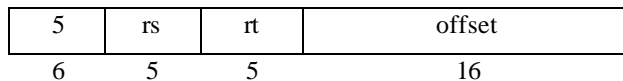
Can't directly load PC with the jump address

4) lui rt, imm



Can't provide Rt as an address to write to the Reg file (mux missing)

5) bne rs, rt, label



Only can branch on equal