

From Algorithms to Systems-on-a-Chip in a Semester

E225C - 2000
Borivoje Nikolic



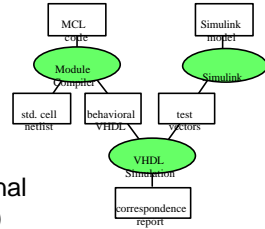
Fall 2000 - EE225C

- Course topics:
 - Communication systems oriented
 - Building blocks
 - Datapaths, arithmetic (adders, multipliers, MACs, dividers, CORDICs)
 - Parallelization, pipelining, unrolling, etc.
 - Transformations: FIR filters, Viterbi decoders
 - Systems
 - Finite wordlengths, ADCs, AGC, adaptive equalizers, sequence detection
 - Applied to xDSL, Gigabit ethernet, wireless, disk drives



Projects

- 18 students
- Two phases:
 - Block design
 - Putting a system together
- Simulink + Module Compiler + functional equivalence (VSS)



Design Projects

- Timing recovery for CDMA
- OFDM receiver with multi-antenna support
- 3G Turbo decoder
- LDPC iterative decoder
- Polyphase filter bank
- RAKE receiver
- Adaptive image-reject mixer
- Decoder for maskless lithography

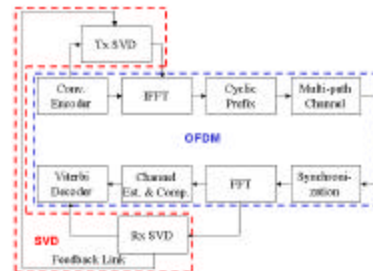


OFDM Receiver

- Similar to 802.11a system specification
- Blocks
 - Synchronization
 - FFT
 - Viterbi decoder
 - SVD
- System Integration and Simulation
- Students: Hayun Tang, Ning Zhang, Dejan Markovic, Yun Chiu

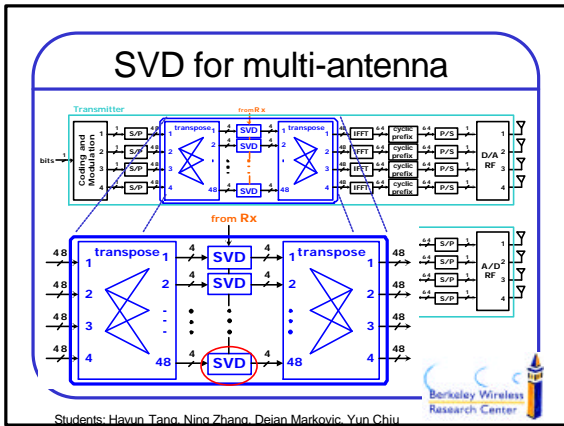


OFDM receiver



Students: Hayun Tang, Ning Zhang, Dejan Markovic, Yun Chiu

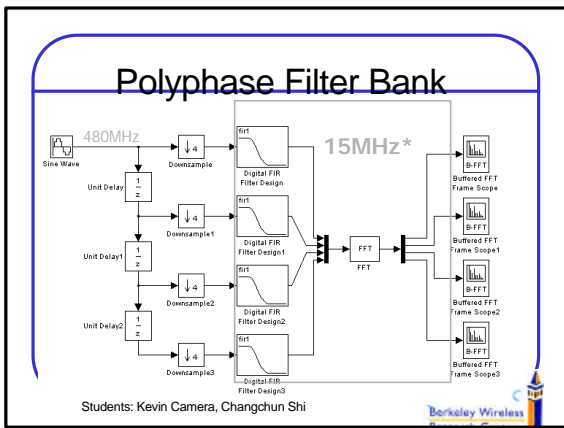
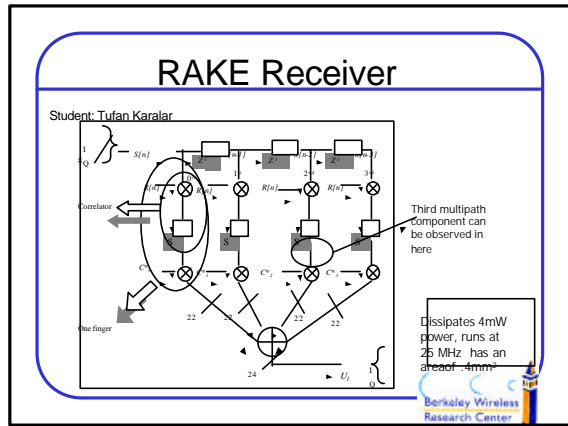
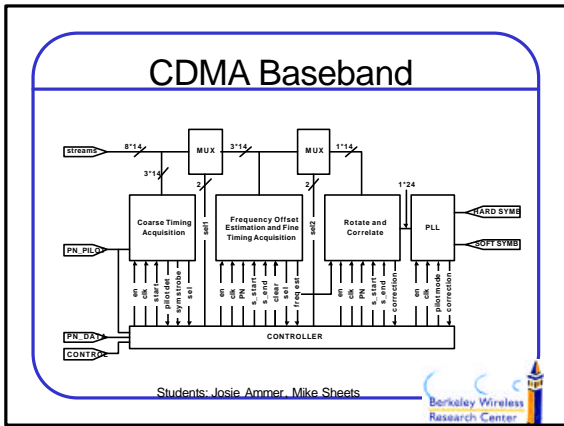




CDMA Baseband

Students: Josie Ammer, Mike Sheets

- Design a 1.6 Mbps DSSS timing recovery unit
- Modulation
 - Length 31 PN code
 - QPSK symbol constellation
- System specifications
 - Maximum frequency offset of +/- 200 KHz
 - Minimum input SNR of +1 dB
 - Input is in-phase & quadrature samples at 200 MHz with 7 bits each



Adaptive Image-Reject Mixer

Image-Rejection Ratio is reduced by circuit mismatches

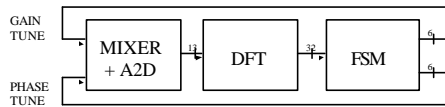
- Phase mismatch in quadrature oscillators
- Gain (DA) mismatch in I and Q paths

Need 60 dB IRR

Students: Gabriel Desjardins, Isaac Sever

Adaptation via Spectral Estimation

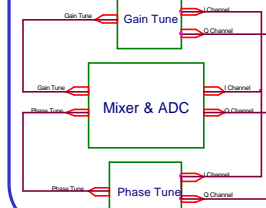
- Two Components
 - Discrete Fourier Transform, Finite State Machine
- FSM uses DFT output to make gain and phase tuning decisions



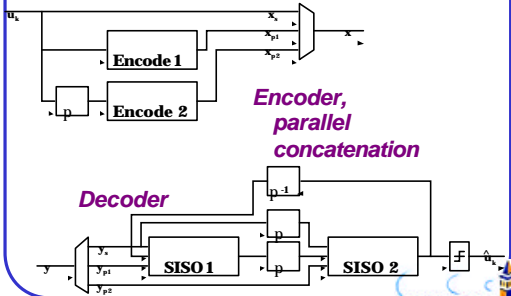
Adaptation via LMS

LMS Update Equation

$$G_{A_{n+1}} = G_{A_n} - n\mathbf{K}_n \mathbf{e}_n$$



3G Turbo Decoder

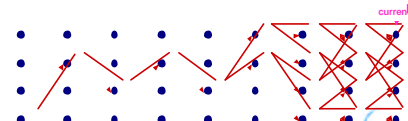


Students: Stephanie Augsburger, Chris Savarese



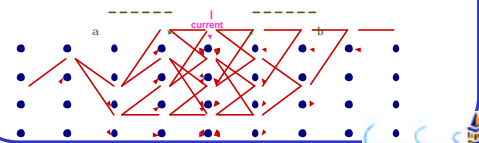
SISO Block: SOVA Implementation

- Standard Viterbi algorithm plus soft output
- Reliability Measure Unit computes soft outputs
- Less complex than MAP
- Expected higher BER than MAP

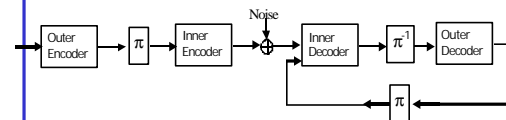


SISO Block: MAP Implementation

- Double Viterbi algorithm: forward and backward
- Soft output is a Log-Likelihood Ratio (LLR)
- More complex than SOVA
- Expected BER improvement over SOVA



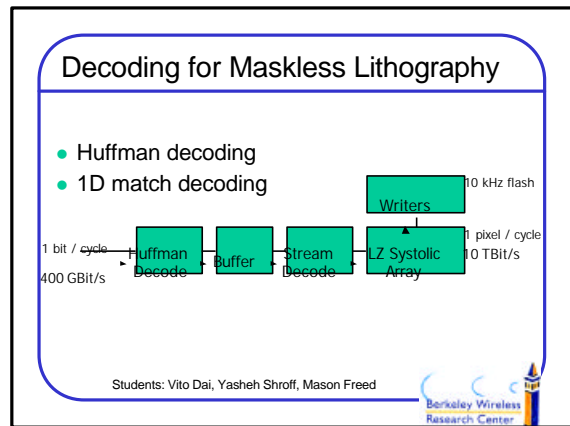
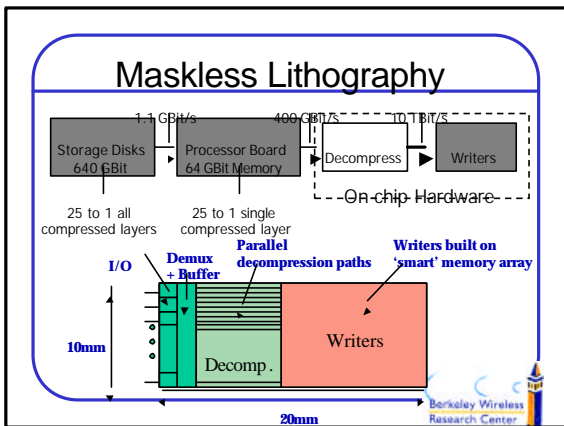
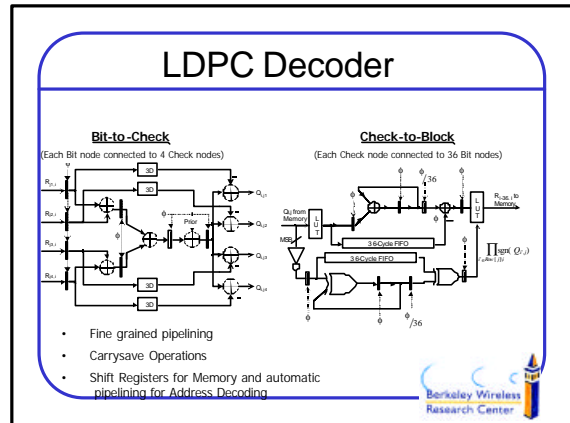
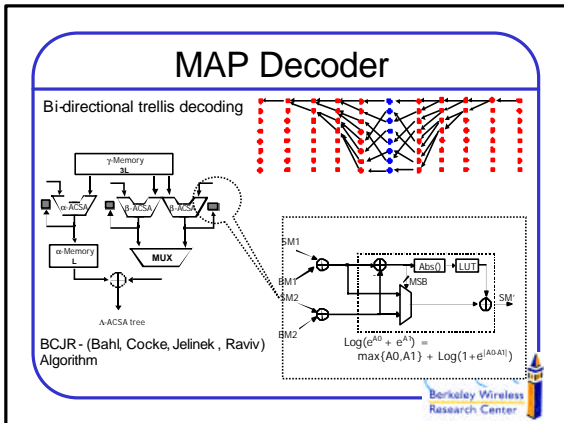
High-Speed Iterative Decoder



Outer: Turbo (convolutional) or Low-density parity-check code
 Inner: Channel with MAP (BCJR) or SOVA decoder

Students: Yeo, Zlatanovic





Separate Class Project

SCF 1
0.25 μ m CMOS
Fully functional first time

SCF 2
Bob Brodersen, Mats Torkelsen, Nathan Chan
Using the new design flow

Berkeley Wireless Research Center

- ### What did we learn?
- Flow works surprisingly well
 - Easy to learn
 - Still fragile
 - Need to add support for SRAM
 - Need block-level timing analysis
 - For faster designs will need regular placement
- Berkeley Wireless Research Center