

EE 225C VLSI Signal Processing

Homework 1

Due on February 12, 2003

1. Floating-point raised cosine filter
 - (a) Using SIMULINK, design a square root raised cosine filter with 3 dB cutoff frequency at 1 MHz and sidelobes of 40dB below the mainlobes using as little taps as possible.
 - (b) Using the chain downloaded from http://bwrc.eecs.berkeley.edu/classes/ee225c/assignments/hw1_Q1.mdl which models a two-tapped channel including sampling offset, and the square root raised cosine filter designed in part 1(a), investigate the effect of tap coefficient and sampling offset on the bit error rate, eye diagram and constellation of a QAM modulated signal.
2. Fixed-point raised cosine filter
 - (a) Using the Xilinx block set, design a fixed-point raised cosine filter meeting the same specification as in part 1(a).
 - (b) Same as part 1(b) but replace the floating-point filter with the fixed-point filter designed in part 2(a). In addition, investigate the effect of finite word length on the bit error rate, eye diagram and constellation of a QAM modulated signal.
3. Realize the fixed-point raised cosine filter designed in part 2(a) using the *delay*, *adder* and *gain* blocks only. Use as little blocks and word length as possible.
4. Implement the filter in Q3 on the BEE, and estimate the area and power consumption.