

EE 225C VLSI Signal Processing

Homework 2

Due on March 5, 2003

1. Architectural tradeoffs

- (a) Calculate the energy efficiency and area efficiency metrics, MOPS/mW and MOPS/mm², for the following four chips that appeared in the 2003 ISSCC.
- (b) Compare their efficiencies with the comparison of ISSCC chips presented in class and discuss where these fit. Explain the results by comparing C_{sw} , V_{dd} and A_{op} .
- (c) For extra credit find a copy of the ISSCC technical digest and find other chips with enough information to calculate the efficiencies and repeat a and b above.

2. High speed FIR filter design

Given a filter order of 8 (9 tap coefficients) and an oversampling rate of 4, design a square-root raised cosine filter with 3 dB cutoff frequency at 1 MHz and maximum sidelobe of 30 dB

Implement the filter using the Xilinx block set using an architecture that has the minimum critical path by using the BEE design flow to get delay estimates for implementation on a Xilinx FPGA. Minimize coefficient word length, with 12 bits for the data. What is the critical path?

3. IIR filter design

- (a) Implement a two pole recursive structure in the Xilinx block set with variable coefficients (i.e. use multipliers and store the coefficients in a register) using the Xilinx block set with 12 bit coefficients and data and an architecture which minimizes the area.

$$y(n) = a_1 * y(n-1) + a_2 * y(n-2) + x(n)$$

What is the iteration bound?

- (b) Implement the filter using an architecture that is as fast as possible. What is your critical path now?