

EE 225C VLSI Signal Processing

Homework 4

Due on April , 2003

The goal of this problem set will be to implement a single carrier, 20 Mbit/sec QPSK transmitter and receiver that uses an equalizer to compensate for the channel impairments. A prototype transceiver with time varying channel (Doppler frequency of 100 Hz) can be downloaded from

<http://bwrc.eecs.berkeley.edu/Classes/EE225C/assignments/hw4.mdl>

that is composed of a data source, modulator and demodulator, raised cosine filters and the time varying channel model with noise as well as the BER calculator, constellation and eye diagram outputs.

- 1) First use high level Simulink blocks (or Matlab) to determine the equalizer algorithm and the exact parameters of your equalizer. You can choose which equalizer structure to use. (If you feel very adventuresome, I can give you some other structures to look at). You can use a training sequence for the equalizer, but make it as short as possible. You can adjust the symbol timing (detection at the maximum point in the eye diagram) to give the best results. Find the minimum channel signal to noise ratio that your system can use that gives an error rate of $1e-3$.
- 2) Implement this equalizer in the Xilinx block set using an architecture that runs as fast as possible as reported by the BEE_ISE tools. (Start with a simple implementation and then improve on its performance as you have time). This will involve not only choosing the right architecture, but minimizing the word length. Don't add more than one dB of implementation loss to the minimum signal to noise ratio you determined in part 1.
- 3) Add the analog impairments model that you developed in problem set 3 and find the signal to noise range over which your receiver can operate and still retain a $1e-3$ bit error rate. Which impairments were most detrimental?