

# EE 225C VLSI Signal Processing

## Homework 5

**Due on April, 2003**

The goal of this problem set will be to implement a single carrier, 20 Mbit/sec QPSK transmitter and receiver that uses a synchronizer to compensate for the channel impairments. A prototype transceiver together with a channel that includes a timing offset, timing drift and frequency offset, can be downloaded from <http://bwrc.eecs.berkeley.edu/Classes/EE225C/assignments/hw5.mdl> that is composed of a data source, modulator and demodulator, raised cosine filters and the out-of-sync channel model with noise as well as the BER calculator, constellation and eye diagram outputs.

1. First use high level Simulink blocks to determine the timing and frequency synchronization algorithms and the exact parameters of your equalizer. You can explore any synchronization algorithms. Here are some suggestions:
  - Preamble for timing synchronization, for example, maximum length shift register (MLSR). See Appendix I.
  - Correlator and possibly amplitude estimator to estimate the timing offset. See Appendix II and sample modules I for possibly useful components.
  - Frequency offset estimation and correction. See Appendix III and sample modules II & III for CORDIC implementation.
  - DPLL-based frequency offset tracking.
  - Data-aided timing drift tracking.Use the shortest preamble while attaining an error rate of  $10^{-3}$  after viable tracking.
2. Implement this synchronization modules in the Xilinx block set.