

## Appendix II (extracted from Peimin Chi's MS thesis)

### Correlator

After differential demodulation, the next task is to correlate against the local preamble. This can be mathematically written as

$$\begin{aligned} q[n] &= \sum_{i=0}^{N-1} r[n-i] * p^*[i] \\ &= \sum_{i=0}^{N-1} (r_I[n-i] + j r_Q[n-i]) * (p_I[i] - j p_Q[i]) \\ &= \sum_{i=0}^{N-1} (r_I[n-i] * p_I[i] + r_Q[n-i] * p_Q[i]) + j (r_Q[n-i] * p_I[i] - r_I[n-i] * p_Q[i]) \end{aligned} \quad (4.2)$$

where  $r[n]$  is the output from the differential demodulator and  $p[n]$  is the preamble, and subscript I indicates real part and subscript Q indicates imaginary part.

#### 4.3.1 FIR-based Correlator

Equation (4.2) shows the correlator can be broken down into four FIR filters with the  $p[i]$ 's as coefficients. The direct way to implement an FIR filter is to delay the input stream, then multiply the delayed tap line by the filter coefficients, and finally sum everything together. With this implementation, an N-tap FIR requires N-1 registers and N multipliers. For the final sum, if only two-input adders are available, then we will need  $\log_2 N$  adders. Table 4.3 lists all the components for the correlator if we directly implement the FIR filter.

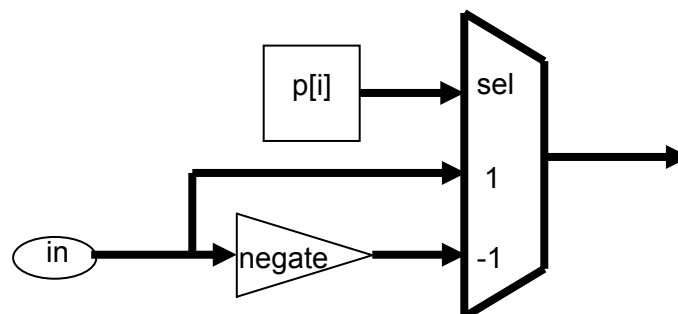
| Elementary Components<br>of Correlator |            |
|--|------------|
| Registers                              | $4(N-1)$   |
| Adders                                 | $4\log_2N$ |
| Multipliers                            | $4N$       |

Table 4.3 Hardware for Direct Implementation of N-tap FIR within Correlator

The large number of basic components, especially multipliers shown in Table 4.3 indicates that the correlator might take large area when implemented. If area is a limited resource, then an alternative way has to be used.

#### 4.3.2 Multiplexer-based Correlator

A closer examination of Equation (4.2) reveals that the coefficients for the FIR filters are that of a PN sequence, which belongs to the set  $\{+1, -1\}$ . We can take advantage of this fact and eliminate all the area-consuming multipliers. This can be done with a multiplexer that takes in preamble  $p[i]$  as the select signal and the input stream and its negate as the two signals to select from. This is shown in Figure 4.2.



### Figure 4.2 Multiplexer-based Correlator

Therefore we have replaced the multipliers with a negate block and a two-input multiplexer. This saves considerable area as a negate block has approximately the same size of an adder and a multiplexer consist of two AND gates and one OR gate. With this approach, the new hardware cost is listed in Table 4.4.

| Elementary Components<br>of Correlator |             |
|--|-------------|
| Registers                              | $4(N-1)$    |
| Adders                                 | $4\log_2 N$ |
| Negate                                 | $4N$        |
| Multiplexers                           | $4N$        |

Table 4.4 Hardware for Multiplexer-based Correlator