UNIVERSITY OF CALIFORNIA

College of Engineering

Department of Electrical Engineering and Computer Sciences

Last modified on October 30, 2000 by Hanching Fuh (hfuh@eecs.berkeley.edu)

Borivoje Nikolic *Homework #7 Solutions* *EECS 141*

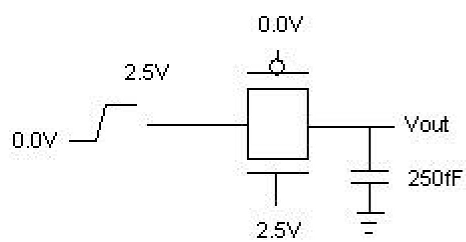
Due Date: Wednesday, October 31, 2000 **(Halloween!)** *at 5:00pm in drop-box outside 275 Cory*

HAPPY HALLOWEEN!

1. Performance of Transmission Gates

As we have learned (or will learn soon!), pass transistors are not ideal switches. Consider the transmission gate below.

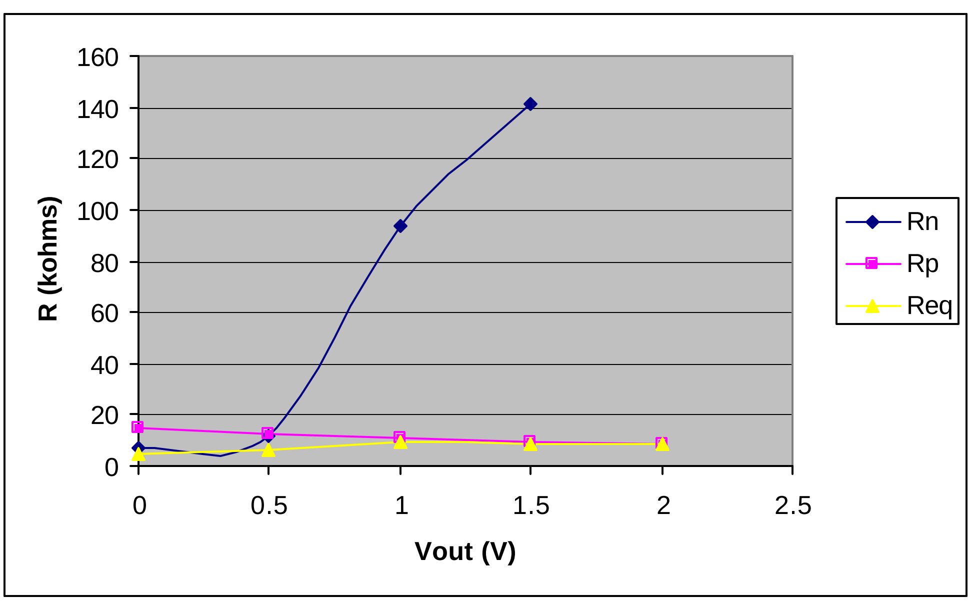
Figure 1: Transmission gate -



The input switches from 0.0V to 2.5V and the transmission gate drives a 250 fF load.

a) Calculate the transmission gate resistances (R_n, R_p, and R_{eq}) in 0.5Vsteps as the output voltage switches from 0.0V to 2.5V. Graph these resistances on the same graph.

Vout (V)	NMOS region	PMOS region	Rn (kohm)	Rp (kohm)	Req (kohm)
0.0	saturation	saturation	6.89	15.1	4.73
0.5	saturation	linear	11.4	12.6	5.99
1.0	saturation	linear	93.8	10.7	9.6
1.5	saturation	linear	141.5	9.47	8.88
2.0	cutoff	linear	infinity	8.58	8.58
2.5	cutoff	linear	infinity	0	0



(Two pieces of advice: 1) Don't forget body effect!; and 2) Equations 6.22 and 6.23 won't work for the whole range!)

Calculations with k_n' = 115e-6, k_p' = -30e-6, W_n = 0.32um, W_p = 0.5 um
Your results may have varied depending on your choice of "minimum" width. You will not be penalized as long as your estimate was reasonable.

b) What is the propagation delay t_p of this gate?

As you calculated, the R_{eq} stays relatively constant over the range of V_{out}. Averaging over the range, R_{eq} is reasonably estimated as 7.5 kohms. Thus, t_p = 0.69 * 7.5kohm * 250fF = **1.3 ns**

2. Happy fun dynamic logic

Dynamic logic is fun! Hopefully you'll still think so after this problem….

a) Implement the following function in dynamic logic: F = ((A+B)C)'
Shown below in Figure 1

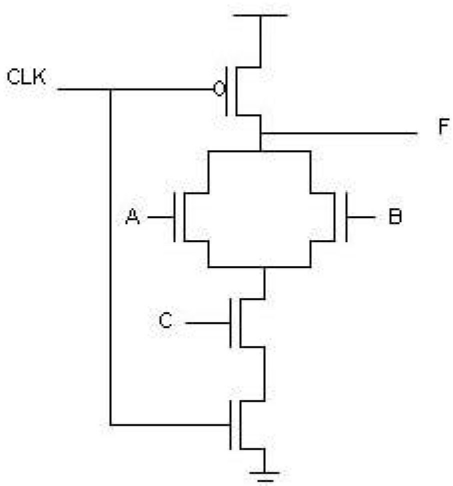


Figure 1: part a

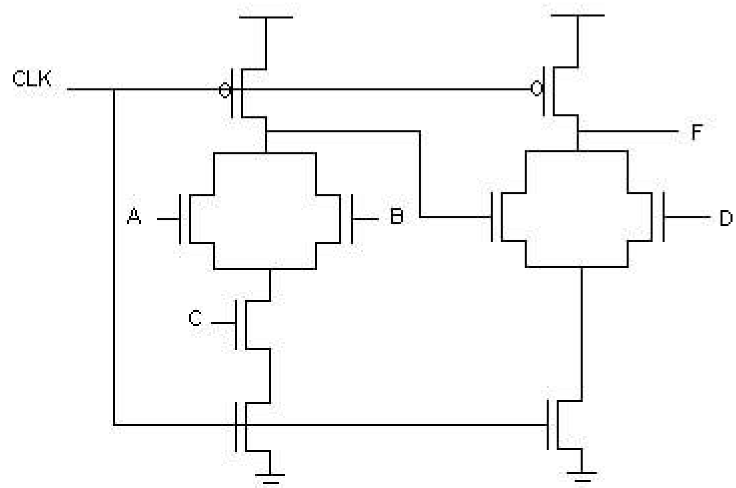


Figure 2: part b

b) Cascade the output of the circuit into a second stage to implement F=[((A+B)C)'+D]'
Shown above in Figure 2

c) Will the circuit in part b work correctly? Why or why not? If not, give an example of when the circuit works incorrectly.
No, it will not work correctly. As we stated in lecture and discussion, precharg-evaluate blocks do not cascade well because of erroneous discharge. An example is whenever it is in precharge, the second stage output state will be indeterminate because the NMOS [with input ((A+B)C)'] is on and the PMOS is on at the same time, fighting for control of the output. Uh oh!

d) The logic function in part b annoys your friendly TA (annoyed TA's give hard problem sets!). Please help me out. I don't like having too many inversions (the ') in a logic function. Write the equivalent function with only one ' in it.
Hint: If you don't understand what I mean, I don't like multiple levels of inversion like (A'+B)' if it is possible to avoid. Think, what does (A'+B)' equal?
(A'+B)' = AB', therefore [((A+B)C)'+D]' = (A+B)CD'

e) Draw a domino implementation of the circuit in part b/d.
Shown below in Figure 3

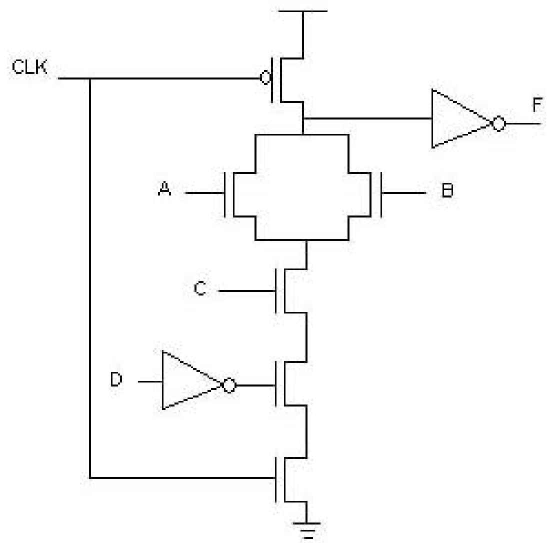


Figure 3: part e

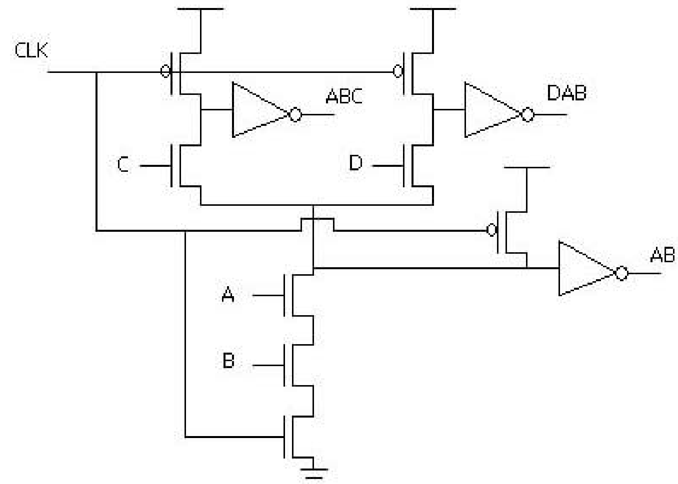
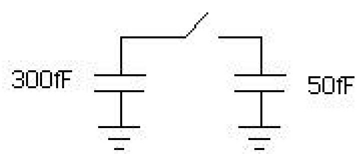


Figure 4: part f

f) This part has nothing to do with the previous parts except it is also a dynamic circuit. Draw a multiple output domino circuit with two outputs: AB and BAC+DAB.
Shown in Figure 4 above

3. The arbitrary problem



a) The 300fF capacitor is initially at 2.5V, while the 50fF capacitor is initially at 1.0V. When the switch is closed, what will the final voltage on each capacitor be? What is the change in energy in energy between the initial and final states?

Total initial charge (remember Q=CV!) = 300fF * 2.5V + 50fF * 1.0V = 8e-13 C
Final voltages across each capacitor is equal = V_{final} = 8e-13 C / (300 fF + 50 fF) = **2.29V**

b) Why do you think we are asking you this question (i.e. what does this have to do with dynamic circuits)?
Why, not? We're fairly arbitrary people, aren't we? In all seriousness, this problem relates to charge sharing, which is a common problem in dynamic circuits and in dynamic RAM (as you will learn later this semester)

We promised an easy problem set this week! I hope you agree… Good luck on your project progress =). No more homework for some time…