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Homework #3: CMOS Inverters and Design Rules

EECS 141

Problem #1

Consider the inverter circuit shown in Figure 1a with an ideal square-wave input. Assume that short-channel effects are negligible – meaning $V_{DSAT} \gg V_{DS}$, $V_{GS} > V_T$.

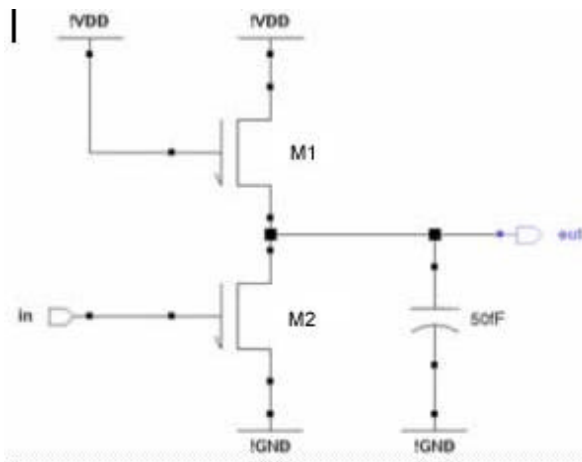


Figure 1a

!VDD = 5.0V
 $V_t = 0.7V$
 $V_m = V_{dd}/2 = 2.5V$
 $L_{M1, M2} = 0.5\mu m$
 $W_{M1} = 0.75\mu m$
 $W_{M2} = 1.0\mu m$
 $L_{diff} = 0.625\mu m$
 $k_n = 100\mu A/V^2$
 $\lambda = 0 V^{-1}$
 $\gamma = 0.2 V^{1/2}$
 $\phi_F = -0.3V$

Reference:
 Table 3.5 (Draft Chapters)
 Draft Chapter 5

(For your own edification, a node preceded by a “!” (i.e. !V_{DD} and !GND) denotes a global node in a netlist.)

Using the information above and references in the text, determine the following:

- a) Find V_{OH} and V_{OL} . Clue: both the load and driver transistors are NMOS, so don't say 5.0V and 0V!
- b) Calculate t_{pLH} and t_{pHL} . This will require you to find a R_{eq} and C_{eq} in each case.
- c) The 50fF load capacitor drawn in the diagram, rather than being an explicit capacitor, actually models the parasitic capacitance. List at least two sources of this parasitic capacitance, as well as two things a design and/or process engineer can do to alter/reduce it. (Hint: What capacitances are inherently present at the output node of this stage? These will be the parasitics!)
- d) Find the static power dissipation for –
 - i. $V_{in} = 0.0V$
 - ii. $V_{in} = 5.0V$

Problem #2

- a) It is always good to get a feel for design rules in a layout editor. Fire up **max** with the mmi25 (0.25 um) technology file (this is the default setup). Place a minimum sized NMOS transistor and examine the dimensions. The layers are listed and shown below in Figure 2a. Determine and list the following:
- Minimum Transistor Length
 - Minimum Transistor Width
 - Minimum Source/Drain Area
 - Minimum Source/Drain Perimeter

Please list the design rules you come across that lead to your results.

**TIPS* - Use Shift-G to access the grid menu. Set the coarse grid to 0.1um, fine grid to 0.01um
Use Shift-Y to explain the design rules within a selected area

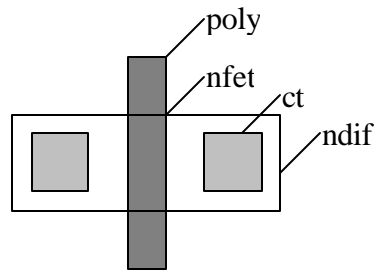


Figure 2a

- b) We desire a minimum sized CMOS inverter with a symmetrical VTC ($V_M = V_{DD}/2$) in the mmi25 technology. Calculate the following for the pull-up PMOS transistor in the design.
- Minimum Transistor Length
 - Minimum Transistor Width
 - Minimum Source/Drain Area
 - Minimum Source/Drain Perimeter

Assume the following:

$V_{DD} = 2.5V$, $V_M = 1.25V$, and refer to Table 3.2 in the Draft Chapters

- c) Using the same minimum size inverter from part b), determine the input capacitance (i.e. the load it presents when driven). Please calculate the capacitance during a transition. From these, determine the total load capacitance that the inverter presents.
**Hint: Consider the Miller effect*
- d) Using the g25 model provided in '[~ee141/MODELS/g25.mod](#)', please verify the accuracy of your results in part c by determining the total input capacitance in a high-low and a low-high transition with HSPICE and comparing with your total capacitance in part c. Turn in your HSPICE input deck.

You'll notice there are four corners, TT, FF, SS, FS, and SF. These represent the different variation extremes we can expect due to process variations. For example, TT stands for NMOS: typical, PMOS: typical. FS stands for NMOS: fast, PMOS: slow etc. For this homework, please use the TT model.

To use these models, include the following in your HSPICE deck:

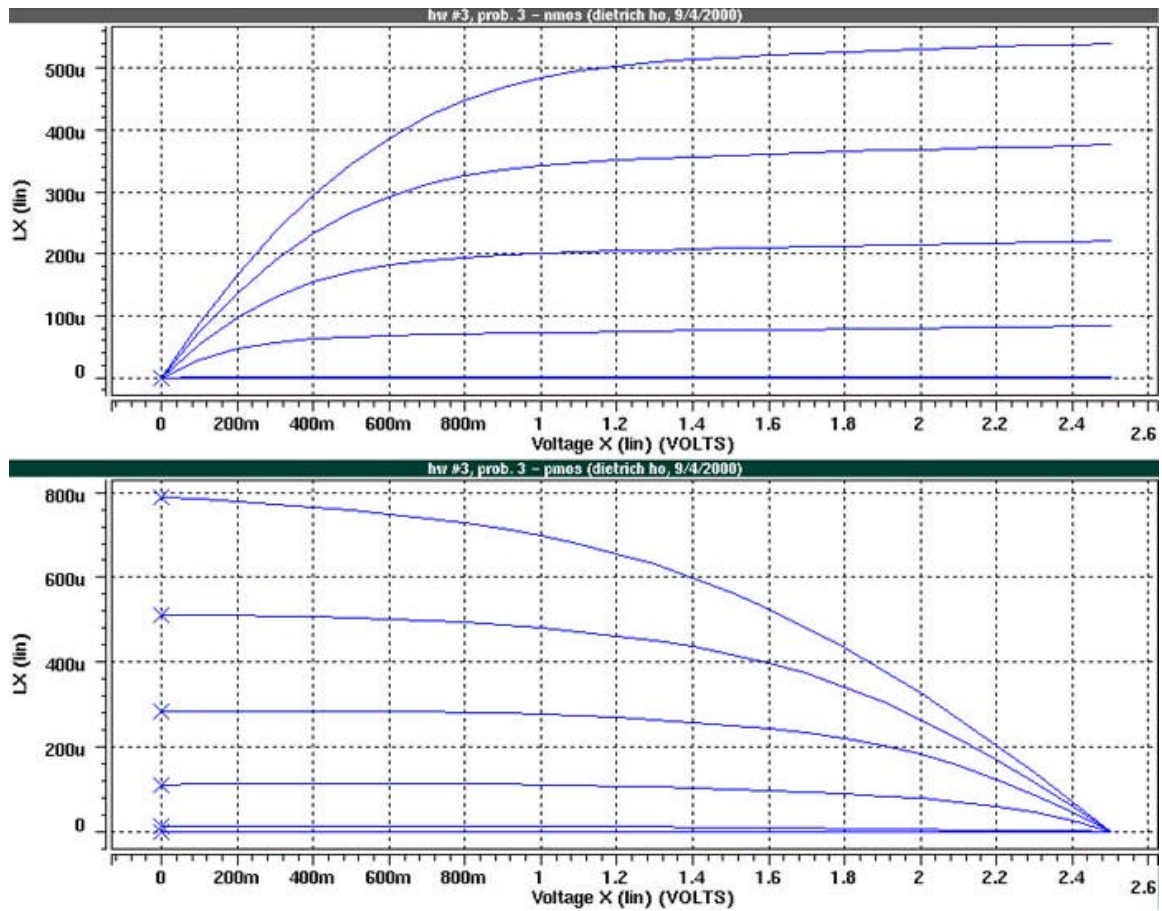
.lib '~ee141/MODELS/g25.mod' TT

- e) Determine V_{IH} , V_{IL} , NM_H , and NM_L .
**Hint: The 2 parameters r and g vary proportionally with transistor width. The equations given are derived with the minimum width in mind. (Please refer to Eq's 5.3 and 5.10 in the draft chapters for r and g)*

Problem #3

- a) Figure 3a depicts the $I_d - V_{OUT}$ curve of a typical NMOS transistor
 Figure 3b depicts the $I_d - V_{OUT}$ curve of a typical PMOS transistor

Assume we use these FETs to create a CMOS inverter. Using this family of curves, graph the VTC, and calculate V_M , V_{IL} , and V_{IH} .



Top: Figure 3a, Bottom: Figure 3b

- b) If we increase the W/L ratio of the pull-down NMOS (leaving the PMOS size fixed), in which direction will the VTC shift?
 c) If instead, we increase the W/L ratio of the pull-up PMOS (and leave the NMOS the original size), in which direction will the VTC shift?
 d) Please explain how the resizing in b) and c) will affect the above I-V curves in each case and give an intuitive explanation of how this affects the VTC of each.