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Borivoje Nikolic *Homework #4: Capacitance, Process Scaling, and Sizing* *EECS 141*

Problem #1: Adiabatic capacitor charging

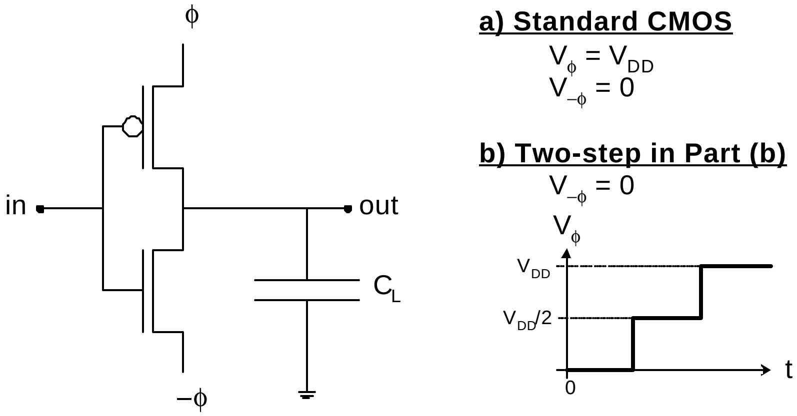

Figure 1: Inverter with Variable Power Rails

Recall that the power consumption of an inverter has two principle components: static power dissipation and dynamic power dissipation. Adiabatic switching is one approach to mitigate these losses. This is accomplished by changing the voltage on the power and ground rails, instead of keeping them constant like in ordinary CMOS logic. Assume $C_L >> C_{INT}$ (ie. intrinsic capacitance is negligible).

a) Consider the transient response of a standard CMOS inverter as shown in Figure 1a (with constant rails at V_{DD} and 0) and external load C_L. Assuming sufficient time for the load capacitance to fully charge/discharge between transitions, how much energy is consumed charging the load for a pull-up (low to high) transition. How much energy is consumed for a pull-down (high to low) transition?

After a pull-up transition, how much energy is stored on the capacitor? Why is this different from the total energy consumed to charge the capacitor?

b) Now, let's see what happens if the power is applied in two steps during a pull-up transition, as shown in Figure 1b. Assume that *in* = 0 and that there is plenty of time between the steps for the capacitor to charge up. How much energy does it take to charge the capacitor all the way up to V_{DD} using this two-step approach?

Derive a simple expression for N steps and make a statement about the energy required as N approaches infinity.

c) In theory, an infinite amount of time is required for a capacitor to fully charge up through a resistance. Clearly, this is too long to wait in a real circuit, so the charging time will be defined as the time it takes for the capacitor to charge up another 90%. Assuming the effective resistance of an 'ON' transistor is R, consider again the two-step charging technique used in Part (b). How long does it take to charge the capacitor from 0 to $0.9*(V_{DD}/2)$? From there (after applying the second step), how long does it take to charge up another 90%? What is the voltage across the capacitor at this point?

Derive a simple expression, as a function of the number of steps N, for the time it takes to charge the capacitor, assuming the capacitor is charged 90% more at each step. Call this the propagation delay of this inverter.

As an interesting aside, the charge could be saved somewhere else when the load capacitance is discharged. Since the charge was saved, a switch could be thrown and everything could run backwards to restore the charge to its original configuration. In this way, the computer consumes almost no energy, and this is the fundamental premise behind ‘reversible computers’.

Problem #2: Process Scaling

A state-of-the-art embedded microprocessor from a company in the valley consumes 0.3mW/MHz when fabricated using a 0.13 µm process. With typical standard cells (gates), the area of the processor is 0.7 mm^2. Assume a 140 Mhz clock frequency, and 1.5 V power supply. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

a) Using fixed voltage scaling and constant frequency, what will the area, power consumption, and power density of the same processor be, if scaled to 0.10 µm technology, assuming the same clock frequency?

b) If the supply voltage in the scaled 0.10 µm part is reduced to 1.2 V, what will the power consumption and power density be? How fast could the scaled processor be clocked? What would the power and power density be at this new clock frequency?

c) Power density is important for cooling the chip and packaging. What would the supply voltage have to be to maintain the same power density as the original processor?

Problem #3: Propagation Delay and Energy

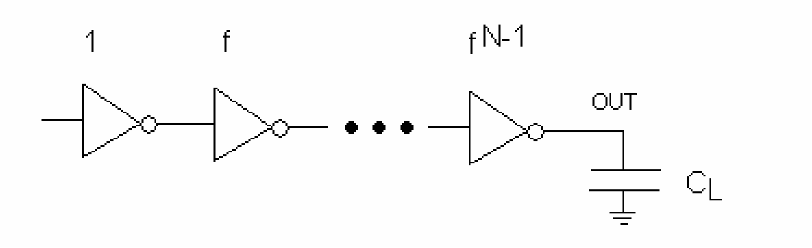

Figure 2: Progressively Sized Inverter Chain

a) What is the delay of a minimum sized inverter driving another inverter *f* times its size? For the minimum sized inverter, assume input capacitance equal to $3C_{unit}$, equivalent resistance through the NMOS or PMOS equal to R_{unit}, and intrinsic (self-loading) capacitance on the output also equal to $3C_{unit}$. Assume that the capacitance and resistance values scale linearly with size. Your answer will be in terms of these parameters (no calculations!). Take the limit as f goes to 0 and call the result τ_{inv}.

b) How much energy is consumed by the driving inverter after successive low to high (L? H) and high to low (H? L) transitions, in terms of a supply voltage Vdd?

c) Consider the chain of N progressively sized inverters shown in Figure 1 (the first is minimum sized). If the output load C_L=96 C_{unit}, what sizing factor f would minimize the total delay for a chain of N=5 inverters? Find the total delay of this chain in terms of τ_{inv}.

d) Find the optimum number of inverters and sizing ratio for the output load specified in Part (c). Express the optimum delay again in terms of τ_{inv}. Considering your result for Part (b), do you think this inverter chain will consume more or less energy than a single inverter driving the output load?