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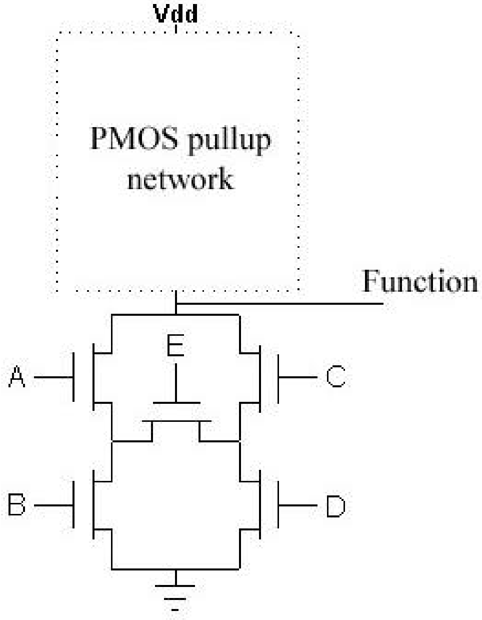
Borivoje Nikolic *Homework #5* *EECS 141*

Problem #1

A two stage buffer is used to drive a metal wire of 1 cm. The first inverter is a minimum size with an input capacitance C_i=10 fF and a propagation delay t_{p0}=175 ps when loaded with an identical gate. The width of the metal wire is 3.6 μm. The sheet resistance of the metal is 0.08 Ω/ÿ, the capacitance value is 0.03 fF/μm^2 and the fringing field capacitance is 0.04 fF/μm.

a. What is the propagation delay of the metal wire?
b. Compute the optimal size of the second inverter as to minimize the total delay. What is this minimum delay through the buffer?

Problem #2



The figure to the left is a logic gate we want to implement in complementary CMOS. As you can see, the gate is already half drawn for you. We've given you the NMOS pull-down network. You'll have to figure out the PMOS pull-up network!

a. What is the logic function of this gate? (F = ???)

b. Using the methods described in the text in the lecture notes, draw the Euler path diagram for both PMOS and NMOS networks.

c. Using your Euler path diagram as a guide, draw the transistor schematic for the NMOS network.

Problem #3

An exclusive-OR (XOR) gate is a very important building block for many digital components (i.e. adders, etc.). We would like to implement it in complementary CMOS.

a. Write down the function table for an XOR and the function (F=???).

b. Looking at the function table, implement EITHER the NMOS or PMOS network. You can even do both if you'd like!

c. Using an Euler path diagram, draw out the full complementary CMOS implementation of the XOR. Don't forget any transistors! (As you can see, complementary CMOS is not an efficient way to implement the XOR. We will teach you better ways to do this soon!)

d. Notice, one path is unnecessary in the XOR. Get rid of it and redraw the XOR to reflect this change. Technically, this implementation is not complementary CMOS, but it is close!

Problem #4

Suppose the EE 141 TAs are your future bosses at work. We are rather arbitrary people and since we are at a low point in the business cycle, we have decided to give all our employees (EE 141 students) a pop quiz. We have decided we would like you to design a three input NOR gate with the same average t_{phl} as a 2.5V, 0.25 μ technology inverter. The inverter has $W_{PMOS} = 2.5\ \mu$ and a symmetrical output swing. Both the inverter and the three input NOR will be driving a 50fF load (ignore other capacitances), but we want to implement the NOR with ratioed logic (Figure 6.24, section 6.2.2). The PMOS width in the NOR gate is the same as the inverter. You are given that all input combinations are equally probable and that you must calculate your answers using the unified model and parameters given in table 3.2 of the reader.

a. Calculation: What are the sizes of the NMOS transistors in the NOR gate to achieve the same average t_{phl} as the inverter?

b. How many truly "unique" ways to pull down the output are there? Write HSPICE code for your NOR gate, simulate the t_{phl} of these unique cases, and graph the results on the same axis. If you're curious, you can simulate all the possibilities, but please don't hand in a graph of all eight!

c. Would the t_{plh} of the NOR be slower, faster, or the same as the inverter? Why?

d. Calculate the V_{OH} and V_{OL} of the NOR gate. How many V_M's exist for the NOR gate? Please calculate the lowest V_M.

e. Problem 6.4: Given the choice between NOR or NAND logic, which one would you prefer for implementation in pseudo-NMOS. Why?