

**Problem #1 – Exercise**

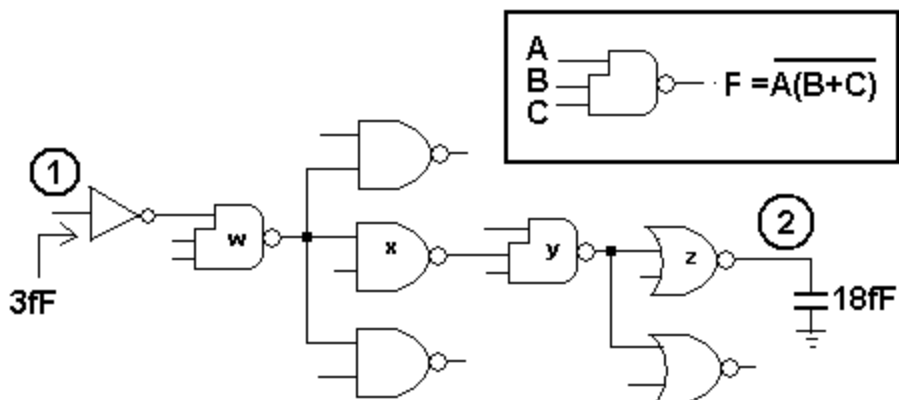
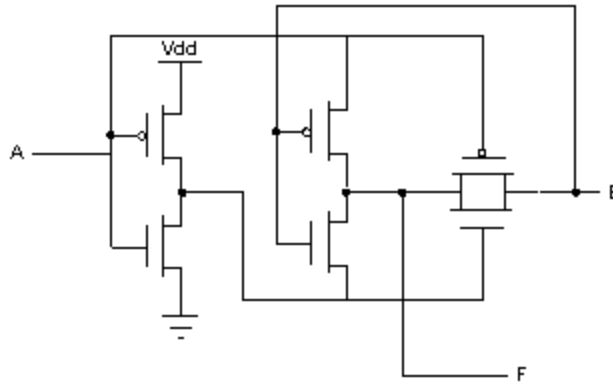


Figure 1. XNORT path.

1. A three-input XNORT gate (see insert above) works like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized inverter (with sizes relative to a minimum sized NMOS). Find the logical effort associated with each input.
2. Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will a XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?
3. Describe how an XNORT gate might be utilized in a 1-bit adder.
4. For the logic path from node (1) to node (2) shown in Figure 1, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?
5. Find the input capacitances  $\{w, x, y, z\}$  necessary for each of the gates in the path in order to achieve the optimum effort per stage.

**Problem #2 – Pass Transmission Gates**

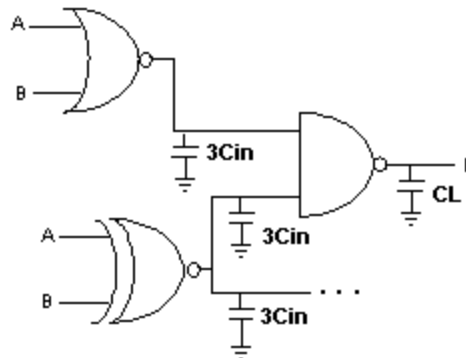
The figure below is a logic gate that also incorporates a transmission gate in between the output node F and input node B.



1. Determine the logic function of this gate. ( $F = \dots$ )

**Problem #3 – Dynamic Power Dissipation**

A simple combinational logic network is shown below.



You may assume that all input combinations are equally likely. Let  $C_{in}=0.8fF$ , and  $C_L=12fF$ .

1. Calculate the activity factor for the output (F) of the network shown above.
2. Calculate the dynamic power consumption if the inputs are switching at rate of 200MHz at a supply voltage of 2.5V.
3. Suppose 200MHz is the maximum frequency at which your design can run. Through extensive simulation, you discover that your maximum clock rate is only 6% lower if you decrease the supply voltage by 10%. By what percentage does the power dissipation of the above circuit decrease under the new conditions?