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**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**  
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Homework #9

EECS 141

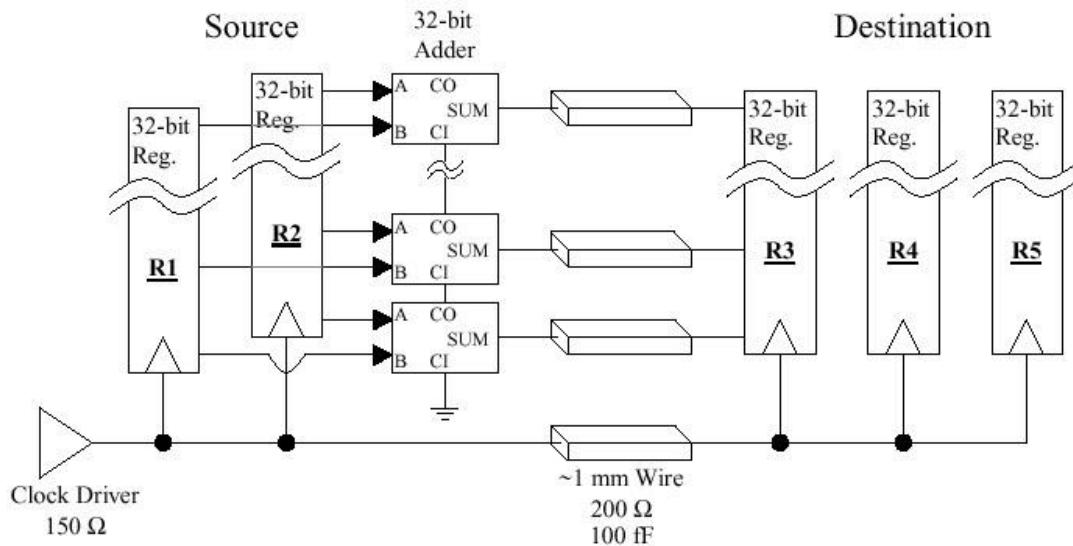
Due Thursday December 6, 2001 at 5:00 PM in drop-box outside of 275 Cory

**This is your LAST homework... Hurray!**

**Problem 1 – Timing & Race Conditions**

The following circuit consists of a source portion, which adds the outputs of two registers R1 & R2 and a destination portion, which stores the sum in R3. The connections between the source and the destination are made by an automatic router, which creates wires with an average length of 1mm and containing an average of 10 contact holes in series. This leads to a resistance of about 200  $\Omega$  and capacitance of about 100 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3 and two other registers (R4 & R5) which happen to be close by. Each register presents a load of 300 fF to the clock driver.



Assume the following timing values for the logic:  $t_{\text{carry}} = 250$  ps,  $t_{\text{sum}} = 300$  ps (including the wire load),  $t_{\text{setup}} = 150$  ps,  $t_{\text{hold}} = 100$  ps,  $t_{\text{clk-Q}} = 50$  ps.

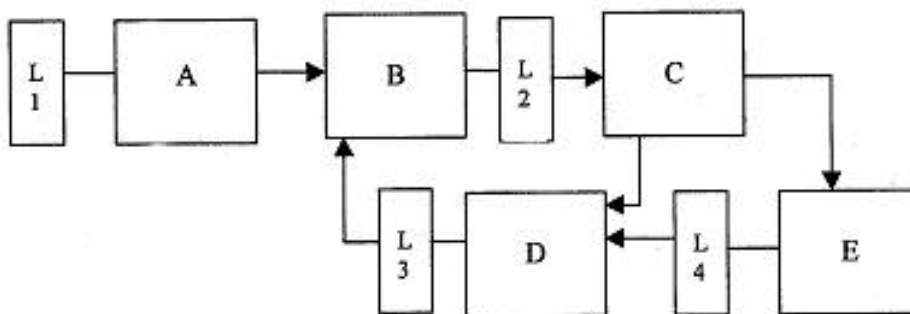
- Does this circuit have a race problem? What is the minimum clock period?
- What if you removed R4 and R5? Would there be a race problem? What would the new minimum clock period be?
- What if the driver were placed at the destination (with R3, R4 & R5)? Would there be a race problem? What would the new minimum clock period be?

## Problem 2 – Timing and Clock Skew

- **Timing and Clock Skew**

3. (4pts) Logic Information. Assume all latches (1-4) are on the same clock and that the logic blocks are static.

$T_{\text{latch}} = 0.3\text{ns}$   
 Block A:  $T_{\text{min}} = 1\text{ns}$   $T_{\text{max}} = 2.1\text{ns}$   
 Block B:  $T_{\text{min}} = 1.7\text{ns}$   $T_{\text{max}} = 2.3\text{ns}$   
 Block C:  $T_{\text{min}} = 0.5\text{ns}$   $T_{\text{max}} = 1.4\text{ns}$   
 Block D:  $T_{\text{min}} = 2.2\text{ns}$   $T_{\text{max}} = 2.9\text{ns}$   
 Block E:  $T_{\text{min}} = 1.5\text{ns}$   $T_{\text{max}} = 3.1\text{ns}$



a.) Determine  $T_{\text{ON,Max}}$ , the maximum time that the clock pulse can be high (i.e. longest time the latches can be open for.) Assume there is NO clock skew.

b.) Determine  $T_{\text{Min}}$ , the minimum clocking period. Once again, assume NO clock skew.

c.) Now assume that the clock is routed from latch 1 (L1) to latch 4 (L4) in ascending order. Assume that the clock skew between subsequent latches is the same (i.e. the skew from L1 to L2 is the same as the skew from L2 to L3). Find the MINIMUM clock skew needed to safely run the clock with a 4.5ns period. Ignoring the duty cycle of the clock for now, what is the MAXIMUM (if any) clock skew allowed such that we can still run the clock with a 4.5ns period?

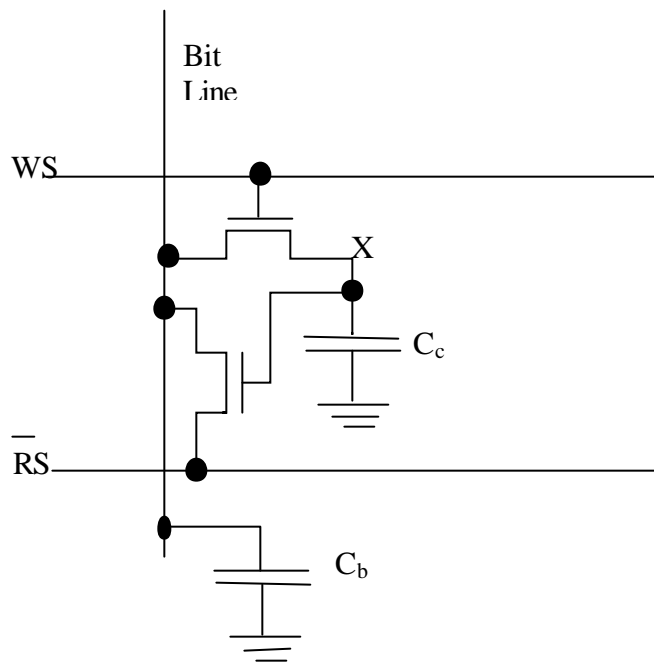
d.) If the clock period is 5ns, what value of clock skew will safely allow the clock to be run at its maximum duty cycle? What is the maximum duty cycle under this condition?

e.) Now, assume that there is a latch (L5) added to the circuit between logic blocks A & B. Also assume that the clock is now routed to the latches in the following order: L1, L5, L2, L4, L3. If the latches are edge triggered, what are the constraints on the clock skew? (Assume no constraints on the clocking period and that the skew between latches is the same.) What is the minimum clock period that can be achieved?

### Problem 3 – Memory Cells

The 2-T memory cell uses 2 identical transistors with  $W/L = 0.3/0.2$ . Separate lines are provided for the read select (RS) and write select (WS), which both switch between 0 and 1.5V. The Bit Line is precharged to  $V_{dd}/2$  prior to a read. A write is done by pulling the Bit Line either to  $V_{dd}$  or to GND. Ignore body effect and channel-length modulation. ( $\gamma=0$ ;  $\lambda=0$ ). Assume for this problem (for ease of calculation) that  $kn' = 110 \mu A/V^2$ ,  $V_{dd}=2.4$ ,  $V_t = 0.4$ .

- Explain the operation of the memory. Draw waveforms for BL, WS, and RS and  $V_x$  for reads and writes of both '1's and '0's.
- Determine maximum current through transistors during a read operation.
- The bit line is connected to a single-ended sense-amp, which would have a switching threshold of 200mV in either direction from  $V_{dd}/2$ . Compute the time required to read a data bit. Assume  $C_c=10fF$  and  $C_b=2pF$ .



### Problem 4 – DRAM Memory Cell

A single-transistor DRAM cell is represented by the following circuit diagram. The bit line can be precharged to  $V_{DD}/2$  by using a clocked precharge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to  $V_{DD}$  or 0V during the WRITE operation with word line at  $V_{DD}$ . Using the parameters given:

$$V_{T0} = 1.0 \text{ V}$$

$$\gamma = 0.3 \text{ V}^{1/2}$$

$$|2\phi_F| = 0.6 \text{ V}$$

- Find the maximum voltage across the storage capacitor  $C_s$  after a WRITE-1 operation, i.e., when the bit line is driven to  $V_{DD} = 5\text{V}$ .
- Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-1 operation after the bit line is first precharged to  $V_{DD}/2$ .

