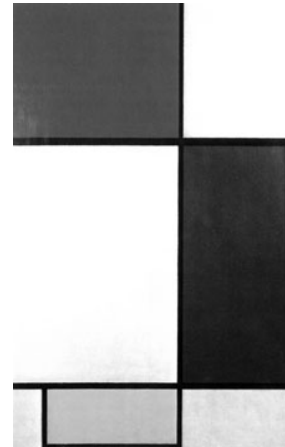


EECS 141 - F01

Lecture 7

Additional Material

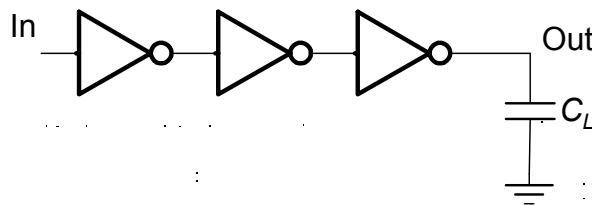


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Inverter Chain



If C_L is given:

- How many stages is needed to minimize the delay?
- How to size the inverters?

May need some additional constraints.

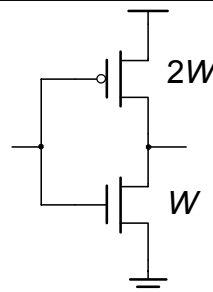
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Inverter Delay

- Minimum length devices, $L=0.25\mu\text{m}$
- Assume that for $W_P = 2W_N = 2W$
 - same pull-up and pull-down currents
 - approx. equal resistances
 - approx. equal rise and fall delays
- Analyze as an RC network



$$R_P = R_{unit} \left(\frac{W_P}{W_{unit}} \right)^{-1} \approx R_{unit} \left(\frac{W_N}{W_{unit}} \right)^{-1} = R_N = R_W$$

$$\text{Delay (D): } t_{pHL} = (\ln 2) R_N C_L \quad t_{pLH} = (\ln 2) R_P C_L$$

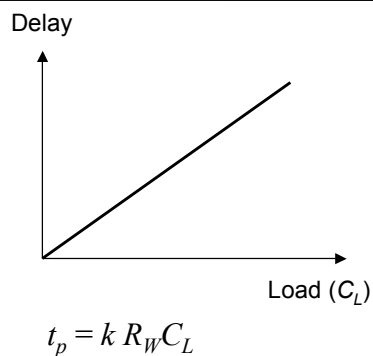
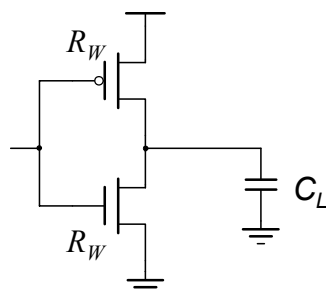
$$\text{Load for the next stage: } C_{in} = 3 \frac{W}{W_{unit}} C_{unit}$$

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Inverter with Load



k is a constant, equal to 0.7

Mead/Conway model: no load - zero delay

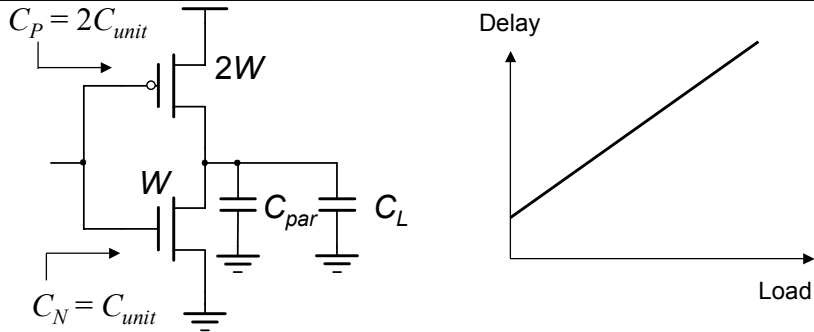
Assume $W_{unit} = 1$

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Inverter with Load



$$\begin{aligned} \text{Delay} &= kR_W(C_{par} + C_L) = kR_W C_{par} + kR_W C_L \\ &= \text{Delay (Internal)} + \text{Delay (Load)} \end{aligned}$$

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Delay Formula

$$\begin{aligned} \text{Delay} &\sim R_W(C_{par} + C_L) \\ &= \frac{R_{unit}}{W}(3\gamma C_{unit}W + C_L) \\ &= 3\gamma R_{unit}C_{unit} + R_{unit} \frac{C_L}{W} \\ &= 3\gamma R_{unit}C_{unit} + R_{unit}C_{unit} \frac{C_L}{C_{in}} \\ &= R_{unit}C_{unit} \left(3\gamma + \frac{C_L}{C_{in}} \right) \\ &= p + g \cdot h \end{aligned}$$

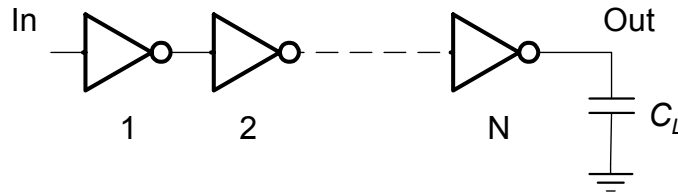
$$h = C_L / C_{in}$$

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Apply to Inverter Chain



$$D = D_1 + D_2 + \dots + D_N$$

$$D_i \sim R_{unit} C_{unit} \left(3\gamma + \frac{C_{i+1}}{C_i} \right)$$

$$Delay = \sum_{i=1}^N D_i \sim R_{unit} C_{unit} \sum_{i=1}^N \left(3\gamma + \frac{C_{i+1}}{C_i} \right)$$

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Optimal Tapering for Given N

Delay equation has $N - 1$ unknowns, $C_2 - C_N$

Minimize the delay, find $N - 1$ partial derivatives

Result: $C_{i+1}/C_i = C_i/C_{i-1}$

Size of each stage is the geometric mean of two neighbors

- each stage has the same effective fanout (C_{out}/C_{in})

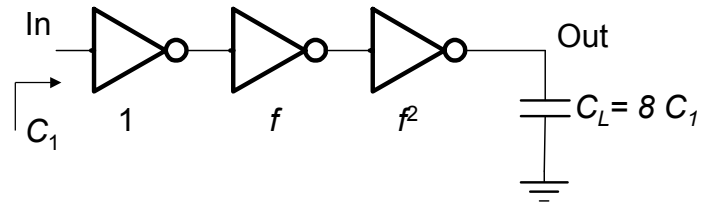
- each stage has the same delay

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Example



C_L/C_1 has to be evenly distributed across $N = 3$ stages:

$$f = \sqrt[3]{8} = 2$$

“Logical Effort”

$$Delay = k \cdot R_{unit} C_{unit} \left(3\gamma + \frac{C_L}{C_{in}} \right)$$

$$= \tau(p + g \cdot h)$$

p – parasitic delay ($3kR_{unit}C_{unit}\gamma$) - gate parameter $\neq f(W)$

g – logical effort ($kR_{unit}C_{unit}$) – gate parameter $\neq f(W)$

h – electrical effort (effective fanout)

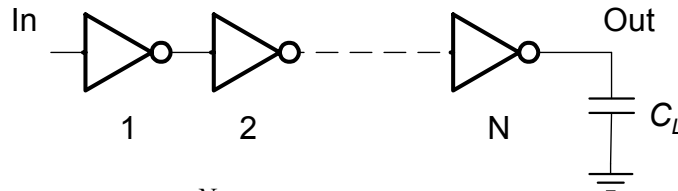
Normalize everything to an inverter:

$$g_{inv} = 1, p_{inv} = 1$$

Divide everything by τ_{inv}

(everything is measured in unit delays τ_{inv})

Buffer Example



$$\text{Delay} = \sum_{i=1}^N (p_i + g_i \cdot h_i) \quad (\text{in units of } \tau_{inv})$$

p_i, g_i are constant (and equal to 1)

Variables are h_i

Minimum delay is when h_i 's are equal
(each stage bears the same effort)

Optimum Effort per Stage

When each stage bears the same effort:

$$\hat{f}^N = F$$

$$\hat{f} = \sqrt[N]{F}$$

Effective fanout of each stage: $h_i = \hat{f}/g_i$

Minimum path delay

$$\hat{D} = \sum (g_i h_i + p_i) = NF^{1/N} + P$$

Optimal Number of Stages

For a given load,
and given input capacitance of the first inverter
Find optimal number of stages and optimal sizing
(Ignore inverting non-inverting)

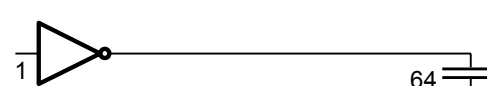
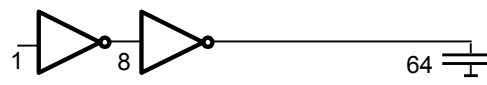
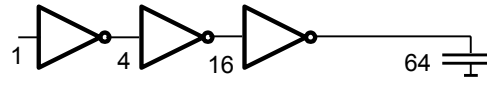
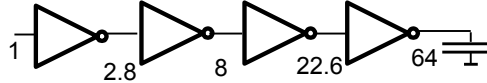
$$\hat{D} = NF^{1/N} + Np_{inv}$$

$$\frac{\partial \hat{D}}{\partial N} = -F^{1/N} \ln(F^{1/N}) + F^{1/N} + p_{inv} = 0$$

Substitute 'best stage effort' $\rho = F^{1/\hat{N}}$

For $p_{inv} = 0$, $\rho = e$

Buffer Design

	N	f	D
	1	64	65
	2	8	18
	3	4	15
	4	2.8	15.3