

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
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FALL 2001 TERM PROJECT PHASE I

EECS 141

Phase 2, due Wednesday, November 21, 3pm.

1. Physical design of a 32-bit adder

In the second phase of the project, you must realize the physical design of the 32-bit adder you designed in phase 1. You should lay out the design using MAX, the layout editor you have become intimately familiar with throughout this semester.

Your layout must be free of design rule errors, and must include wells and sufficient contacts to the wells. Note that the latest version of MAX provides the easy generation of contacts, vias, and wells through the **via** p-cell normally located in the right subwindow of the layout editor. Each input, output, and supply rail should be brought to the edge of the pr-boundary with poly or any of the metal layers.

As with any layout assignment, you will quickly discover that drawing a layout is much simpler if you plan things out ahead of time. It is much easier to have a general layout strategy than to just blindly draw objects on the screen. For example, it is important to plan out how you will distribute the supply and ground rails in your design. As discussed in the labs, we suggest that you draw them horizontally in metal 1. A design that is very regular can easily be tiled and reused, saving you a lot of time. **MODULAR DESIGN IS NECESSARY FOR THE SUCCESS OF THIS PROJECT!!!**

Plan ahead: develop a top-level plan of your design. Try to determine optimal routing and placement of wires. Use common sense in laying out your circuit and remember that long transistors must be built properly. Plan your cells accordingly. We suggest that you use a fixed cell height that can accommodate some integer number of metal 1 wires routed horizontally. Implement different cell sizes by adjusting their width. Plan in advance how you will use your metal wiring in higher levels.

2. Updating Results

Most likely, mapping your design into a physical implementation will cause some important changes in the energy and delay of your circuit. However, the functional operation shouldn't change! You must ensure that your layout and schematic are functionally equivalent by performing LVS (layout-versus-schematic). You must therefore perform both a full functional and performance analysis on your extracted layout.

The goal of this phase of the project is to compare the results before and after physical design, not to improve on the design goals. Explain any major deviations from your results in Phase I. Try not to make any significant changes (i.e. adder architecture, etc.) to your original design of

Phase I. You may make minor modifications to the circuit that do not change the underlying foundation of your design. If you find it absolutely necessary to alter a major part of your circuit (because of non-functionality or unacceptable results), a full motivation should be provided in the report.

Changes in the design goal are NOT allowed!

3. Report

Your report for this phase of the project serves to accomplish two things: 1) You should discuss your overall layout strategy and how it is related to your original design goals. 2) Compare your results in this phase to those that you obtained in the first phase of the project, including any changes you made to the design.

The total report should not contain more than two pages. You are **NOT** allowed to add any other sheets, except for important plots. Use the following guidelines to govern your report content and length:

- Page 1: Executive summary, overall design decisions, remarks, and motivations.
- Page 2: Appropriate layouts, with labeled terminals.

In addition to the report, you must electronically submit the extracted SPICE input deck used to obtain the energy analysis to ee141-project@bwrc.eecs.berkeley.edu. Remember, the quality of the report is major factor in deciding your final project grade for this phase. Please submit a printed copy of your report to the EECS141 drop box.

Grading Scheme

Phase 2 is worth 30% of the total grade on the project. (Phase 1 is worth 40%, and Phase 3 is worth the remaining 30%) Your Phase 2 grade is divided evenly between your general approach and correctness (50%), and the quality of your report (50%).

Frequently Asked Questions

Q: Remember that automatic layout generator we used for the SUE lab...?

A: Don't even think about it. You must design the cell and its constituent sub-cells completely by hand. You will often find that the automatic layout generator does a lousy job. I would be very surprised if you got anything to work with the layout generator.

Q: Our design in Phase 1 was pretty low energy, so I was wondering if I could switch from Speed optimization to Energy optimization.

A: No. You must stick with your original design goals. No exceptions.

Q: My report is a little over 2 pages, and I would like to print EVERY single one of my schematics so you can see the detail in my cells.

A: Use some common sense. If it takes you more than two pages to explain everything, you must be doing a lousy job. As for the layout, just print the main cell as large as you can on the page. We really just want to see that your design is regular or has some structure. We can verify the “greatness” of your design when we run your SPICE decks through our simulators.