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6:00-7:30pm

EECS 141: FALL 2002—MIDTERM 2

For all problems, you can assume the following transistor parameters (unless mentioned otherwise):

NMOS:

$$V_{Tn} = 0.4, k'_n = 115 \mu\text{A}/\text{V}^2, V_{DSAT} = 0.6\text{V}, \lambda = 0, \gamma = 0.4 \text{ V}^{1/2}, 2\Phi_F = -0.6\text{V}$$

PMOS:

$$V_{Tp} = -0.4\text{V}, k'_p = 30 \mu\text{A}/\text{V}^2, V_{DSAT} = -1\text{V}, \lambda = 0, \gamma = -0.4 \text{ V}^{1/2}, 2\Phi_F = 0.6\text{V}$$

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GRAD/UNDERGRAD	
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SOLUTIONS!!!

Problem 1: ____/16

Problem 2: ____/12

Problem 3: ____/10

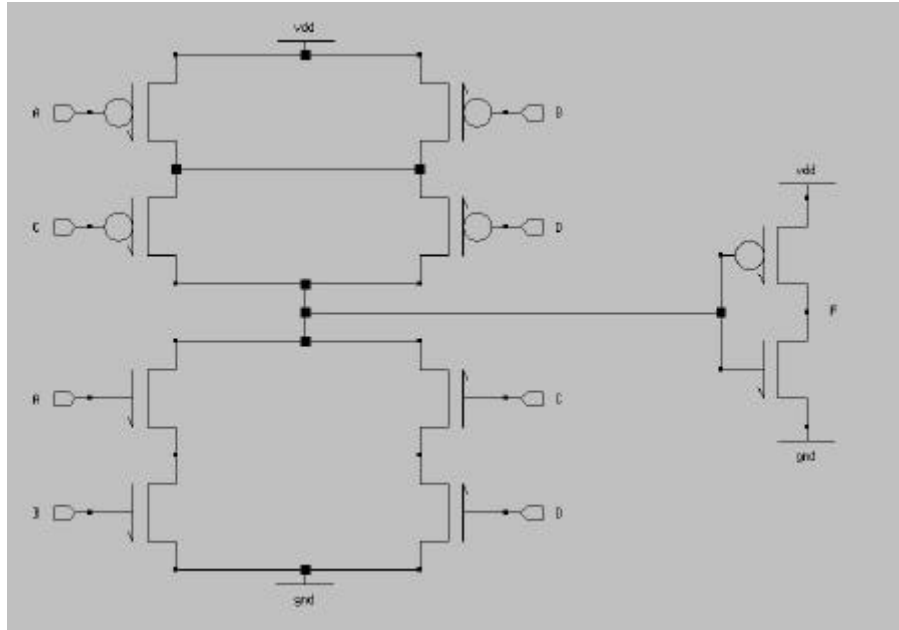
Problem 4: ____/ 6

Total: ____/44

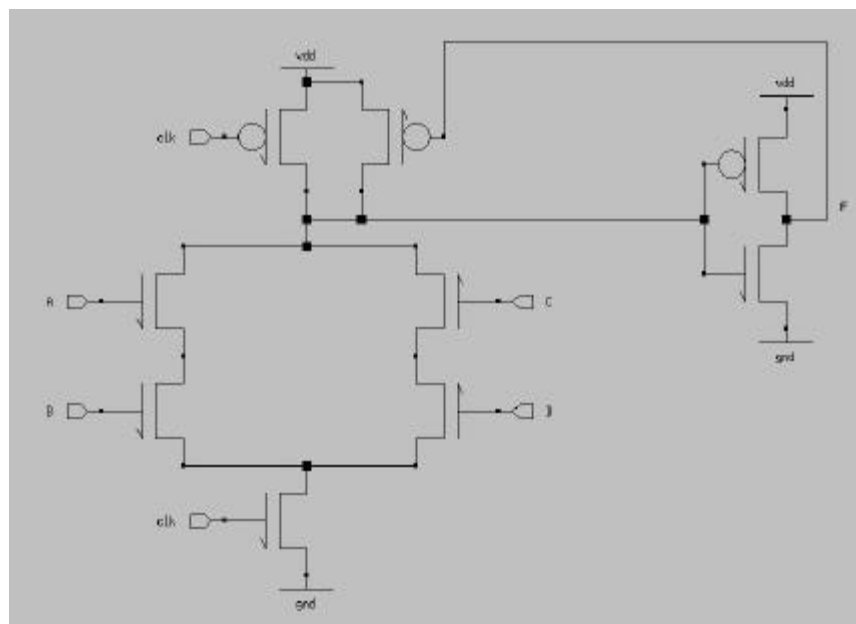
PROBLEM 1. Logic Styles (16pts)

In this problem, for single-ended logic styles, assume that only true inputs are available, and for differential logic styles you can use both true and complementary inputs. Draw a gate implementing $Y = AB + CD$ in:

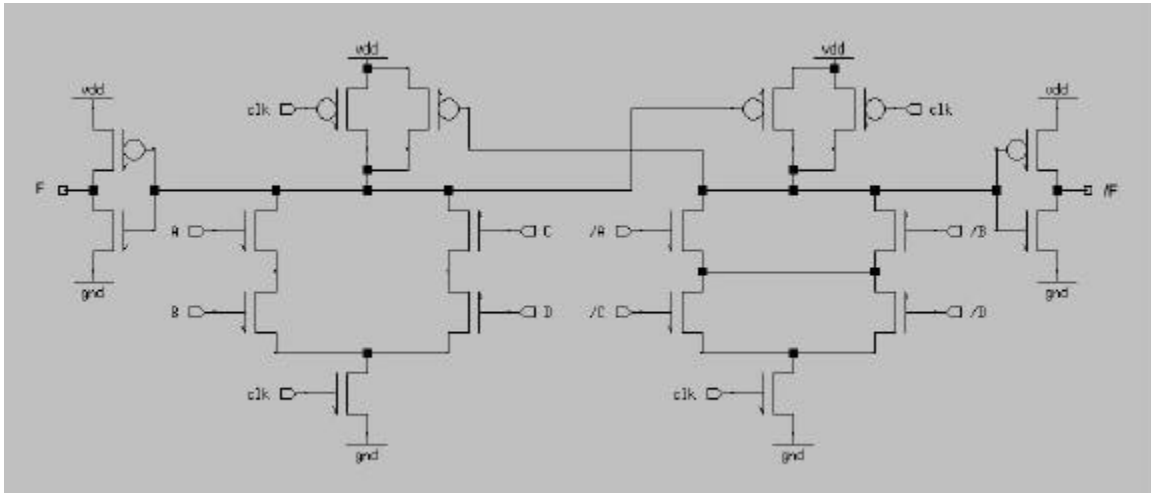
- a) Standard complementary CMOS.



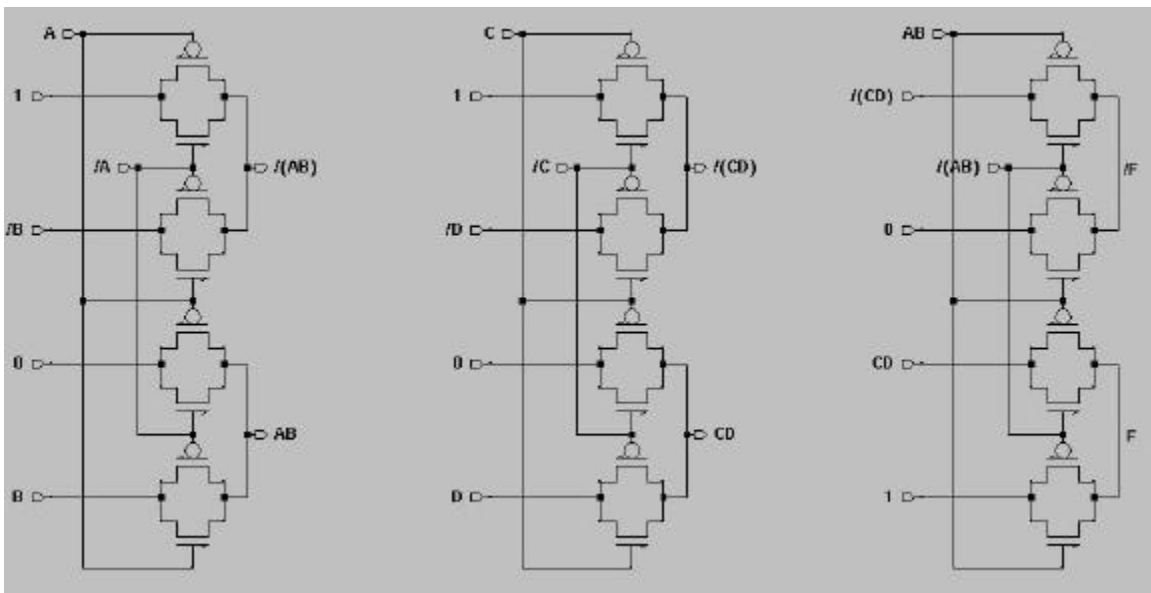
- b) Domino logic.



c) Dual-rail domino.



d) Transmission-gate logic (differential logic style)



PROBLEM 2. Logical effort. (12pts)

- a) (4pts) Find the logical effort for a domino buffer from the figure. Assume that the static inverter is appropriately skewed.

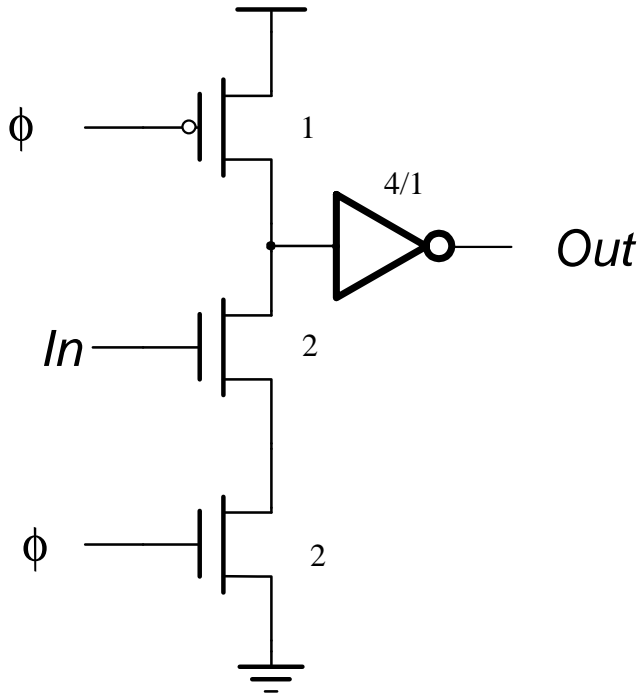


Fig. 1.

Because this is a dynamic circuit, we only care about the evaluate stage – i.e. we only worry about the pull-down network of the dynamic inverter and the pull-up network of the static inverter.

For the first stage (dynamic inverter), $g_1 = 2/3$

For the second stage (static inverter), $g_2 = 5/6$

Total logical effort:

$$g = g_1 g_2 = 5/9$$

$g = 5/9$

b) (8pts) Calculate the optimal fanout for the domino buffer with a foot switch (as one shown in Fig.1).

(Hint: we calculated that the optimal fanout for the static complementary CMOS is about 4. Recalculate this for the domino buffer that consists of a dynamic inverter and a non-skewed static inverter).

First, we must remember that we can size the dynamic and static buffers as separate stages...which means that we are dealing with groups of two stages. Thus, for a given buffer chain, we can find the “average” g and p seen in each stage:

$$p = \frac{p_1 + p_2}{2} = \frac{1 + \frac{5}{6}}{2} = \frac{11}{12} \qquad g = \sqrt{g_1 g_2} = \frac{\sqrt{5}}{3}$$

Now, we can derive the optimal fanout just as we did in class:

$$D = N(p + gf) = \frac{\ln F}{\ln f} (p + gf)$$

$$\frac{dD}{df} = \ln F \frac{g \ln f - \frac{p}{f} - g}{(\ln f)^2}$$

The optimum value of f is when this derivative is zero. Thus we get the condition:

$$\ln f = \frac{p}{gf} + 1$$

Plugging in our g and p , we find:

$$f = 3.77$$

This f is, of course, the capacitance ratio (referred to as h in the lecture notes). If we want the fanout, we just need to compute gf .

$$gf = \frac{\sqrt{5}}{3} \cdot 3.77 = 2.8$$

Optimal fanout = 2.81

PROBLEM 3: Arithmetic Circuits (10pts)

Consider an implementation of a bit-sliced 32-bit carry-lookahead adder implemented in static CMOS. The bit slice is 18 metal pitch, and the metal pitch is 1 μ m. You can assume that the resistance of all metal layers is 0.1 Ω /?. The table below shows the dependence of the intra-layer capacitance per unit length for the metal layer that is used for implementation of this carry wire.

Spacing	Min	1.5 * Min	2 * Min	2.5* Min	3 * Min or more
Capacitance	80aF/ μ m	60aF/ μ m	50aF/ μ m	45aF/ μ m	40aF/ μ m

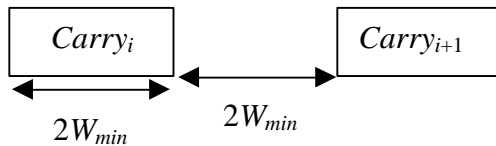
- a) (2pts) How many bit slices does the longest carry wire cross in radix-2 implementation?

The wire in the last carry-lookahead stage spans half the tree, or 16 bit slices.

- b) (2pts) How many bit slices does the longest carry wire cross in radix-4 implementation?

Since this is a 32-bit adder, you could have assumed either a 4x4x2 tree or a 4x2x4 tree. The first tree will be faster, since the carry crosses only 16 bit slices.

- c) (2pts) What is the worst-case coupling capacitance of the wire when all the carries are routed vertically with double-width, double-spaced pitch?



$$C_{total} = 200\text{aF}/\mu\text{m}$$

50 aF/ μ m * 2 for Miller Effect * 2 neighboring wires

- d) (2pts) How does this capacitance change if the wire pitch is doubled from the previous case, without changing the wire width?

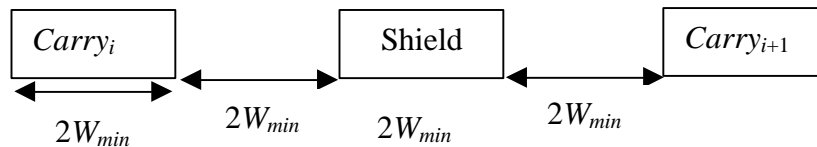
$$C_{total} = 160\text{aF}/\mu\text{m}$$

Pitch = 8* W_{min}

Spacing = 8* W_{min} - 2* W_{min} = 6* W_{min}

40 aF/ μ m * 2 for Miller Effect * 2 neighboring wires

- e) (2pts) If the shielding wires are introduced in the same layer as shown before, what is the worst-case coupling capacitance?



$$C_{total} = 100\text{aF}/\mu\text{m}$$

No Miller Effect: 50aF/ μ m * 2 neighboring wires

PROBLEM 4. Power dissipation (6 pts).

Compute the probability of the energy consuming transitions of the output, F of the logic function $F = \overline{A + B \cdot C}$, implemented in standard static CMOS, if the input probabilities are $p(A=1) = 0.2$, $p(B=1) = 0.5$, $p(C=1) = 0.1$.

The truth table for function F is as follows:

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

The inputs probabilities are as follows:

$$p(A = 1) = 0.2 \Rightarrow p(A = 0) = 1 - 0.2 = 0.8$$

$$p(B = 1) = 0.5 \Rightarrow p(B = 0) = 1 - 0.5 = 0.5$$

$$p(C = 1) = 0.1 \Rightarrow p(C = 0) = 1 - 0.1 = 0.9$$

We now calculate the probabilities for the output to be 1 and 0 using the truth table:

$$p(F = 1) = p(A = 0) \cdot p(B = 0) \cdot p(C = 0)$$

$$+ p(A = 0) \cdot p(B = 0) \cdot p(C = 1)$$

$$+ p(A = 0) \cdot p(B = 1) \cdot p(C = 0)$$

$$= 0.76$$

$$p(F = 0) = 1 - p(F = 1) = 1 - 0.76 = 0.24$$

The probability p of energy consuming transitions of the output is equal to

$$p = p(F = 0) \cdot p(F = 1) = 0.24 \cdot 0.76 = 0.1824$$