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PROBLEM 1 (EULER PATHS AND LOGICAL EFFORT):

1. F = ! ((a * b) + (c * (d + e))) Draw the complementary CMOS circuit that implements this function. Size it such that it has the same pull-up/pull-down strength as a minimum sized 2/1 inverter.
2. Draw (or fire up MAX and draw it there) the layout that would share the most diffusions (do not worry about the correct transistor widths). Show the Euler Path used to arrive at your solution.
3. For the sizing used in part 1, find the logical efforts (g) of the gate for all 5 of the inputs. Are they the same or different?
4. Resize the circuit such that it has the same strength as a 4/1 (skewed-HI) inverter. What are the logical efforts of the gate for each of the 5 inputs now?

PROBLEM 2 (DESIGN WITH LOGICAL EFFORT):

Your circuit requires an 8-input AND gate. Each input may have at maximum an input capacitance equal to twice that of a minimum sized 2/1 inverter (so it can at most present a total unit width = 6). The AND gate needs to drive a load 100 times the input capacitance of a 2/1 inverter (so a total unit width = 300). Thus, this circuit has an electrical effort (H) = 300/6 = 50. Your library has four different 8-input AND gates and each of their critical paths are as follows:

a. 2-input-NAND – INV – 4-input-NAND – INV

b. INV – 4-input-NOR – 2-input-NAND – INV

c. 2-input-NAND – 2-input-NOR – INV – 2-input-NOR

d. INV – 2-input-NOR – 4-input-NAND – INV

(Parasitic Delays: INV (1), n-input-NAND (n), n-input-NOR (n))

Find the delay of each of the four circuits using logical effort (use a spreadsheet or anything to keep track of the numbers. This problem isn't hard—just bookkeeping). Which one is the fastest? Draw out the fastest implementation of the 8-input-AND gate and size them such that the optimal performance is achieved. Why (or why not) does a four-stage AND make sense given the load constraint of this problem?

PROBLEM 3 (COMBO LOGIC AND LOGICAL EFFORT)

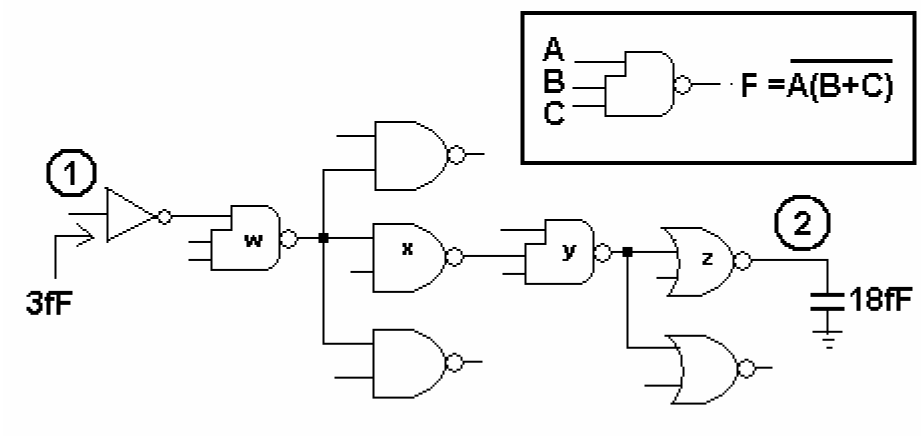

Figure 1 XNORT path.

1. A three-input XNORT gate (see insert above) works like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort associated with each input.

2. Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will a XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?

3. For the logic path from node (1) to node (2) shown in Figure 1, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?

4. Find the input capacitances {w, x, y, z} necessary for each of the gates in the path in order to achieve the optimum effort per stage.