

**UNIVERSITY OF CALIFORNIA**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**  
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*Borivoje Nikolic*

**FALL 2002 TERM PROJECT PHASE I**

*EECS 141*

Phase 2, due Tuesday, December 3, 9am.

## **1. Physical design of a 32-bit adder**

In the second phase of the project, you must realize the physical design of the complete 32-bit adder you proposed in phase 1. You should complete the schematic in SUE, and lay out the design using MAX, the layout editor you have become intimately familiar with throughout this semester, using the cells designed in the first phase.

Your schematic and layout should be well organized, and easy to understand. Your layout must be free of design rule errors, and must include wells and sufficient contacts to the wells. Note that the latest version of MAX provides the easy generation of contacts, vias, and wells through the **via** p-cell normally located in the right subwindow of the layout editor.

As with any layout assignment, you will quickly discover that drawing a layout is much simpler if you plan things out ahead of time. It is much easier to have a general layout strategy than to just blindly draw objects on the screen. For example, it is important to plan out how you will distribute the supply and ground rails in your design. As discussed in phase 1, we suggest that you draw them horizontally in metal 1. A design that is very regular can easily be tiled and reused, saving you a lot of time.

Plan ahead: develop a top-level plan of your design. Try to determine optimal routing and placement of wires. Use common sense in laying out your circuit and remember that long transistors must be built properly. Plan your cells accordingly. You can modify them slightly from phase 1 if they don't fit your top-level floorplan.

Use the same specifications for the height of the bit-slice as you had in phase 1. Arrange the bit slices accordingly, and connect the power and ground. Make your wiring plan: in which metal layers are you going to route long carries? Use metal layers 1-4 for all routing, metal 5 should be used only for routing the bus on the top level. Make sure that you properly strap the supply rails, and that you distribute the clocks if you are using dynamic logic.

## **2. Updating Results**

Most likely, mapping your design into a physical implementation will cause some significant changes in the energy and delay of your circuit. However, the functional operation shouldn't change! You must ensure that your layout and schematic are functionally equivalent by performing LVS (layout-versus-schematic) check. You must therefore perform both a full functional and performance analysis on your extracted layout.

The goal of this phase of the project is to compare the results before and after physical design, not to improve on the design goals. Explain any major deviations from your results in Phase I. Try not to make any significant changes (i.e. adder architecture, etc.) to your original design of Phase I. You may make minor modifications to the circuit that do not change the underlying foundation of your design. If you find it absolutely necessary to alter a major part of your circuit (because of non-functionality or unacceptable results), a full motivation should be provided in the report.

### **3. Simulation**

You should simulate the netlist extracted from your layout, with signals and loading specified as in phase 1. You will report the delay, area and power of your extracted design and compare them to your estimates from phase 1.

### **4. Report**

Your report for this phase of the project serves to accomplish two things: 1) You should discuss your overall layout strategy and how it is related to your original design goals. 2) Compare your results in this phase to those that you obtained in the first phase of the project, including any changes you made to the design.

The total report should not contain more than two pages. You are **NOT** allowed to add any other sheets, except for important plots. Use the following guidelines to govern your report content and length:

- Page 1: Summary of the performance of your design, estimates from phase 1 and extracted data from phase 2.
- Page 2: Executive summary, overall design decisions, floorplan, remarks, and motivations.
- Page 2: Layout of your adder, with labeled terminals.

Also, you should prepare the poster containing 9 slides, that you will present to the class on December 3.

In addition to the report, you must electronically submit the extracted SPICE input deck used to obtain the energy analysis to [ee141-project@bwrc.eecs.berkeley.edu](mailto:ee141-project@bwrc.eecs.berkeley.edu). Remember, the quality of the report is major factor in deciding your final project grade for this phase. Please submit a printed copy of your report to the EECS141 drop box.

## **Grading Scheme**

Phase 2 is worth 50% of the total grade on the project. (Phase 1 is also worth 50%). Your Phase 2 grade is divided evenly between your general approach and correctness (50%), and the quality of your report (50%).