

**UNIVERSITY OF CALIFORNIA**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

*Last modified on September 11, 2003 by Nuntachai Poobuapheun (nuntachp@eecs.berkeley.edu)*

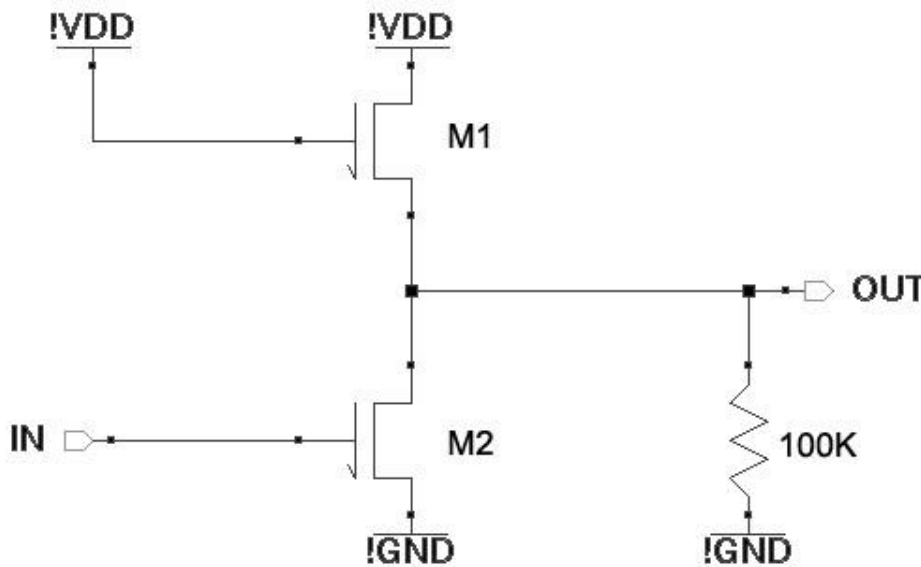
*Borivoje Nikolic*

*Homework #3: CMOS Inverters and Design Rules*

*EECS 141*

**Problem #1**

Consider the inverter circuit shown in Figure 1a with an ideal square-wave input. Assume that short-channel effects are negligible – meaning  $V_{DSAT} \gg V_{DS}$ ,  $V_{GS} - V_T$ .



$V_{DD} = 2.5V$   
 $V_t = 0.5V$

$L_{M1, M2} = 0.25\mu m$   
 $W_{M1} = 2.0\mu m$   
 $W_{M2} = 1.0\mu m$   
 $L_S = 0.25\mu m$   
 ( $L_{diff} = L_S$  for this homework when calculating capacitance.)

$k_n = 100\mu A/V^2$   
 $\lambda = 0 V^{-1}$   
 $\gamma = 0.2 V^{1/2}$   
 $\phi_F = -0.3V$

Use Table 3.5 to find capacitances.

*Figure 1a*

(For your own edification, a node preceded by a “!” (i.e. !V<sub>DD</sub> and !GND) denotes a global node in a netlist.)

Using the information above and references in the text, determine the following:

- a) Find  $V_{OH}$  and  $V_{OL}$ . Clue: both the load and driver transistors are NMOS, so don't say 2.5V and 0V!
- b) Calculate  $t_{pLH}$  and  $t_{pHL}$ . This will require you to find a  $R_{eq}$  and  $C_{eq}$  in each case. There's no explicit load so we'll consider the self loading (only internal capacitances) that is seen at the output (there should be two components).
- c) Assuming a normal pmos/nmos inverter is the load presented at the output, what other capacitances would we have to account for in the  $C_{eq}$  calculation in addition to those you used for part b)?
- d) Find the static power dissipation for –
  - i.  $V_{in} = 0.0V$
  - ii.  $V_{in} = 2.5V$

## Problem #2

- a) It is always good to get a feel for design rules in a layout editor. Fire up Micromagic **max** with the mmi25 (0.25 um) technology file or Cadence Virtuoso with 0.24um technology. Place a minimum sized NMOS transistor and examine the dimensions. The layers are listed and shown below in Figure 2a.
- 2a. Determine and list the following:
- Minimum Transistor Length
  - Minimum Transistor Width
  - Minimum Source/Drain Area
  - Minimum Source/Drain Perimeter

Please list the design rules you come across that lead to your results.

\*TIPS - (Micromagic) Use Shift-G to access the grid menu. Set the coarse grid to 0.1um, fine grid to 0.01um

Use Shift-Y to explain the design rules within a selected area

Refer to Lab2 for Cadence

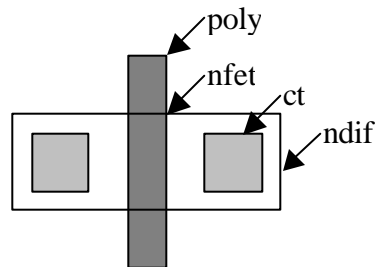


Figure 2a

- b) We desire a minimum sized CMOS inverter with a symmetrical VTC ( $V_M = V_{DD}/2$ ) in the mmi25 technology. Calculate the following for the pull-up PMOS transistor in the design.
- Minimum Transistor Length
  - Minimum Transistor Width
  - Minimum Source/Drain Area
  - Minimum Source/Drain Perimeter

Assume the following:

$V_{DD} = 2.5V$ ,  $V_M = 1.25V$ , and refer to Table 3.2 in the Book

- c) Using the same minimum size inverter from part b), determine the input capacitance (i.e. the load it presents when driven). Please calculate the capacitance during a transition. From these, determine the total load capacitance that the inverter presents.
- \*Hint: Consider the Miller effect
- d) Using the g25 model provided in '[~ee141/MODELS/g25.mod](#)', please verify the accuracy of your results in part c) by determining the total input capacitance in a high-low and a low-high transition with HSPICE and comparing with your total capacitance in part c). Turn in your HSPICE input deck.

You'll notice there are four corners, TT, FF, SS, FS, and SF. These represent the different variation extremes we can expect due to process variations. For example, TT stands for NMOS: typical, PMOS: typical. FS stands for NMOS: fast, PMOS: slow etc. For this homework, please use the TT model.

To use these models, include the following in your HSPICE deck:

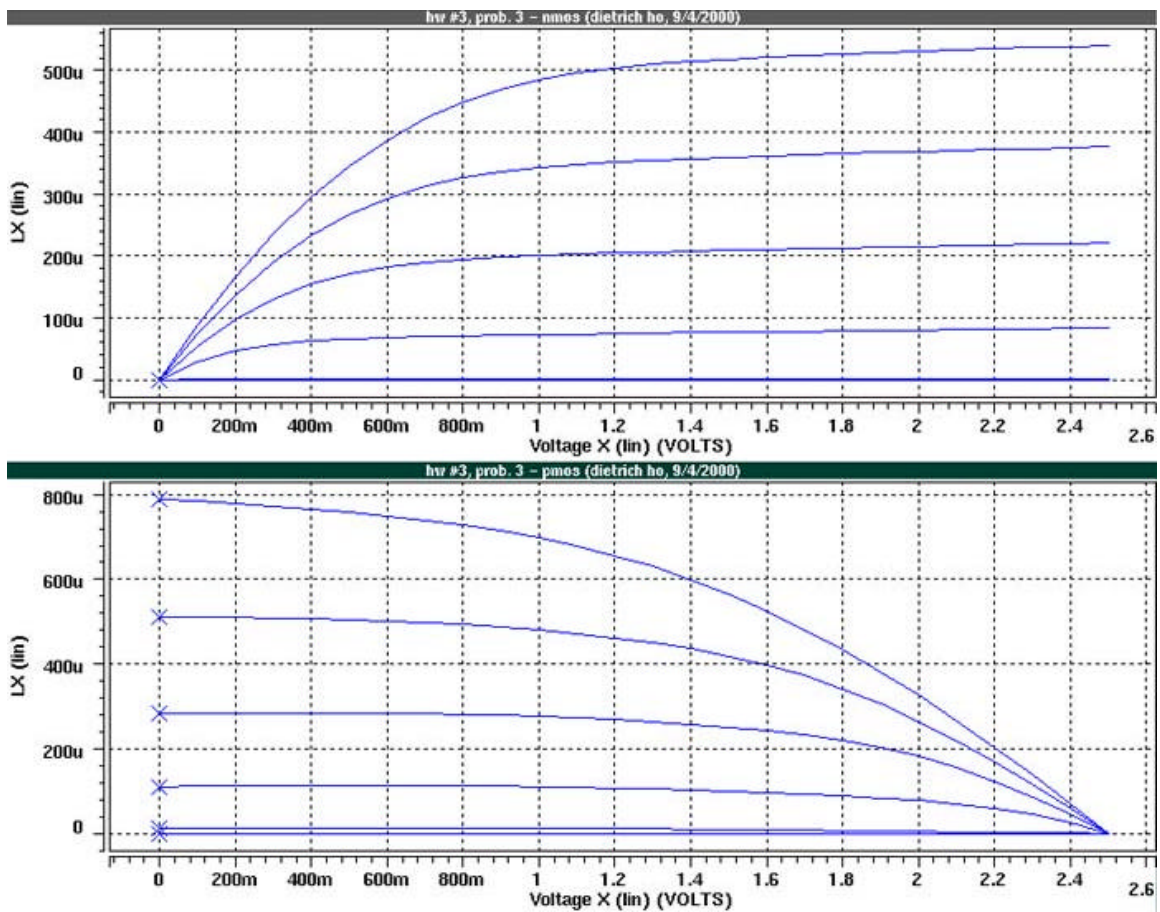
**.lib '~ee141/MODELS/g25.mod' TT**

- e) Determine  $V_{IH}$ ,  $V_{IL}$ ,  $NM_H$ , and  $NM_L$ .
- \*Hint: The 2 parameters  $r$  and  $g$  vary proportionally with transistor width. The equations given are derived with the minimum width in mind. (Please refer to Eq's 5.3 and 5.10 in the book for  $r$  and  $g$ )

### Problem #3

- a) Figure 3a depicts the  $I_d - V_{OUT}$  curve of a typical NMOS transistor  
 Figure 3b depicts the  $I_d - V_{OUT}$  curve of a typical PMOS transistor

Assume we use these FETs to create a CMOS inverter. Using this family of curves, graph the VTC, and calculate  $V_M$ ,  $V_{IL}$ , and  $V_{IH}$ . The values for  $V_{GS}$  you should use are 0, 0.5, 1, 1.5, 2, 2.5 (negative values for the PMOS). There are actually 6 graphs per device, the 0 and 0.5 graphs lay pretty much on top of each other since the current is near 0 for those gate values. These are normal PMOS and NMOS devices so the  $V_{DS}$  values for the PMOS should actually be negative as well as the current. They were just displayed this way so it would be easier for you to work on them.



Top: Figure 3a, Bottom: Figure 3b

- b) If we increase the W/L ratio of the pull-down NMOS (leaving the PMOS size fixed), in which direction will the VTC shift?  
 c) If instead, we increase the W/L ratio of the pull-up PMOS (and leave the NMOS the original size), in which direction will the VTC shift?  
 d) Please explain how the resizing in b) and c) will affect the above I-V curves in each case and give an intuitive explanation of how this affects the VTC of each.

#### Problem#4

An old implementation of MOS inverters is shown in Fig. 4a, in which a diode connected NMOS transistor is used as the load. The standard inverter implementation is shown in Fig. 4b.

We are going to compare them on performance metric. Assume that both of them are driven by a standard inverter (the high input voltage is  $V_{dd}$  and low input voltage is 0). There is a capacitive load  $C_L=150\text{fF}$  on the output node of each inverter, which is large compare to the parasitic capacitances of the devices.

- For inverter A, prove that when the output voltage characteristics satisfy the following relation:  $V_M \approx (V_{OH} + V_{OL})/2$ , the delay for output to rise from  $V_{OL}$  to  $V_M$  (or fall from  $V_{OH}$  to  $V_M$ ) can be modeled as  $t_p = 0.69R_{eq}C_L$ , even if the output swing is not rail – to – rail. Here  $R_{eq}$  is the equivalent resistance of the device driving the output, and  $C_L$  is the load capacitance on the output node.
- Evaluate the propagation delays of the two inverters by measuring the delay as the time between  $V_{IN} = V_M$  and  $V_{OUT} = V_M$ . You will need to find  $V_M$ ,  $V_{OH}$  and  $V_{OL}$  for each of these two inverters first. Use the switch approximation analysis of the MOS transistor presented in class ( $R_{eq} = (R_M + R_{VOH}) / 2$ ) to estimate  $t_{pLH}$ , and same for  $t_{pHL}$ .
- Verify  $t_{pLH}$  and  $t_{pHL}$  using HSPICE. (Note that there may be slight difference between your SPCE and hand calculation results, because approximations are used in our hand analysis. You can think about the reason for the discrepancy while you are not required to do so in this homework.)
- Explain why M2 is sized to be much smaller than M1 in the first (all-NMOS) circuit? Briefly comment on that. What disadvantages on performance does the inverter with NMOS-load have compared to the CMOS inverter?

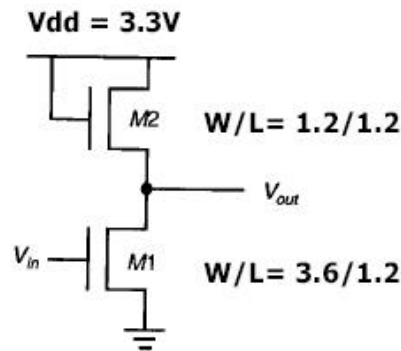


Figure 4a

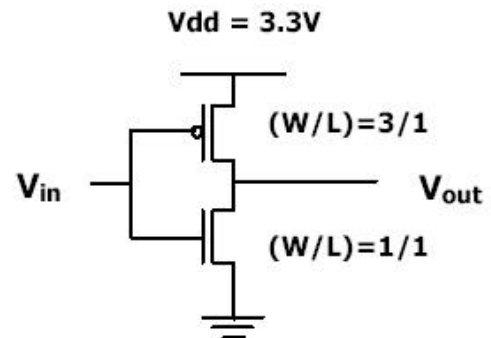


Figure 4b

Use the following parameters:

NMOS:  $V_{T0}=0.6\text{V}$ ,  $k'=20\mu\text{A}/\text{V}^2$ ,  $\gamma=0.5\text{V}^{1/2}$ ,  $\lambda=0.05\text{V}^{-1}$ ;  
 PMOS:  $V_{T0}=-0.6\text{V}$ ,  $k'=7\mu\text{A}/\text{V}^2$ ,  $\gamma=0.5\text{V}^{1/2}$ ,  $\lambda=0.1\text{V}^{-1}$