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Borivoje Nikolic *Homework #4: Capacitance, Process Scaling, and Sizing* *EECS 141*

Problem #1: Adiabatic capacitor charging

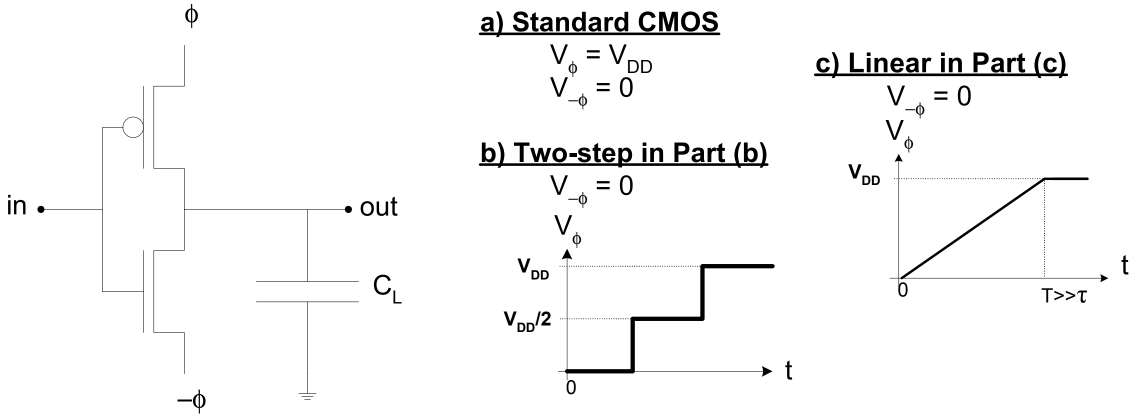

Figure 1a: Inverter with Variable Power Rails

Recall that the power consumption of an inverter has two principle components: static power dissipation and dynamic power dissipation. Adiabatic switching is one approach to mitigate these losses. This is accomplished by changing the voltage on the power and ground rails, instead of keeping them constant like in ordinary CMOS logic. Assume $C_L >> C_{INT}$ (ie. intrinsic capacitance is negligible).

a) Consider the transient response of a standard CMOS inverter as shown in Figure 1a (with constant rails at V_{DD} and 0) and external load C_L. Assuming sufficient time for the load capacitance to fully charge/discharge between transitions, how much energy is consumed charging the load for a pull-up (low to high) transition. How much energy is consumed for a pull-down (high to low) transition? After a pull-up transition, how much energy is stored on the capacitor? Why is this different from the total energy consumed to charge the capacitor?

b) Now, let's see what happens if the power is applied in two steps during a pull-up transition, as shown in Figure 1b. Assume that *in* = 0 and that there is plenty of time between the steps for the capacitor to charge up. How much energy does it take to charge the capacitor all the way up to V_{DD} using this two-step approach?
Derive a simple expression for N steps. Show that the power dissipation will be minimum when each step is equal to Vdd/N for N steps charging.

c) Consider now the linear increase of the supply voltage, illustrated in Figure 1c. Assume that $T >> \tau = RC$ and *in* = 0. How much energy does it take to fully charge the capacitor (to V_{DD})? Can you intuitively explain your result? Why is it no longer valid without the assumption that $T >> \tau$?
Verify your result using your result in (b).

As an interesting aside, the charge could be saved somewhere else when the load capacitance is discharged. Since the charge was saved, a switch could be thrown and everything could run backwards to restore the charge to its original configuration. In this way, the computer consumes almost no energy, and this is the fundamental premise behind 'reversible computers'.

Problem #2: Process Scaling

A not very state-of-the-art embedded microprocessor from a company outside the valley consumes 0.72mW/MHz (excluding leakage power) when fabricated using a 0.18 μm process. With typical standard cells (gates), the area of the processor is 2 mm^2. Assume a 600MHz clock frequency, and 1.8V power supply. Its leakage power is 50μW. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

a) Power density is important for cooling the chip and packaging. Scale the circuit so, that the power density decreases to 150mW/mm^2 but the current density remains constant. What is the new frequency of the circuit?

b) Go now back to the original processor and calculate the scaling required for the circuit to dissipate 0.54mW/MHz. If there are many ways to do that, choose the one that gives maximum frequency without affecting the power density more than 20%. What is the die area of the new circuit?

c) If the threshold voltage in the 0.18μm process is 0.4V, what should be the threshold voltage in 0.13μm process with 1.3V supply voltage? Assuming 90mV/dec subthreshold slope, what would be the leakage power of the new processor?

Problem #3: Propagation Delay and Energy

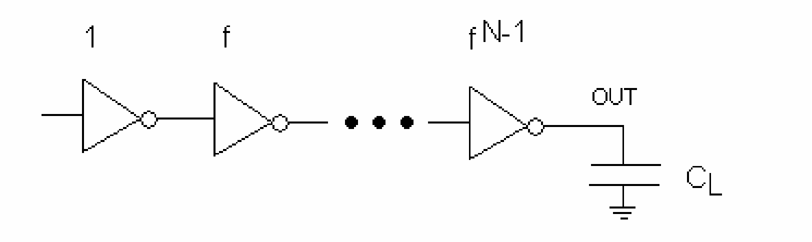

Figure 3a: Progressively Sized Inverter Chain

a) What is the delay of a minimum sized inverter driving another inverter *f* times its size? For the minimum sized inverter, assume input capacitance equal to C_{unit}, equivalent resistance of the NMOS or PMOS equal to R_{unit}, and intrinsic (self-loading) capacitance on the output also equal to C_{unit}. Assume that the capacitance and resistance values scale linearly with size. Your answer will be in terms of these parameters (no calculations!). Take the limit as f goes to 0 and call the result τ_{inv}.

b) From part a), how much energy is consumed by the driving inverter after successive low to high (L→H) and high to low (H→L) transitions, in terms of a supply voltage Vdd?

c) Consider the chain of N progressively sized inverters shown in Figure 3a (the first is minimum sized). If the output load C_L=40C_{unit}, what sizing factor f would minimize the total delay for a chain of N=5 inverters? Find the total delay of this chain in terms of τ_{inv}.

d) Find the optimum number of inverters and sizing ratio for the output load specified in Part (c). Express the optimum delay again in terms of τ_{inv}. Considering your result for Part (b), do you think this inverter chain will consume more or less energy than a single inverter driving the output load?

Problem#4: Buffer Sizing

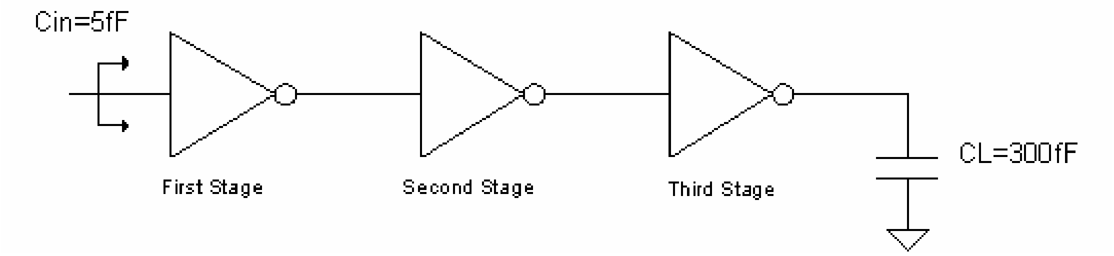

Figure 4a: Buffer Chain

In order to drive a large capacitance (C_L=300fF) from a minimum size gate (with input capacitance C_{in}= 5fF), you decided to introduce a two-stage buffer as shown in Fig. 4a. Assume that the propagation delay of a minimum size inverter is 20ps (for minimum size inverter delay in this case, there is only intrinsic (self-loading) capacitance on the output, which is equal to input capacitance –there is no other output loading). Also assume that the capacitance and resistance values scale linearly with size.

a) Determine the sizing of the two additional buffer stages that will minimize the propagation delay. What is the corresponding propagation delay?

b) Given a supply voltage of 2.5V and activity factor of 0.5, what is the average energy-delay product of the circuit in part (a)?

c) Determine the sizing of the two buffer stages that will minimize the average energy per transition while maintaining the propagation delay within 10% of the minimum value from part (a). For simplicity, assume that sizes are increasing in geometric fashion (1, f, f^2). This means that effective fanout of the first two stages (Cin2/Cin and Cin3/Cin2) is f, while the effective fanout of the last stage is equal to CL/Cin3. What is the new average energy-delay product?

d) Now go to the circuit in Fig.4b. Suppose that there is a 50fF wire capacitance between the second stage and the third (output) stage. What are the sizes of the two buffers in this case that will minimize the propagation delay?

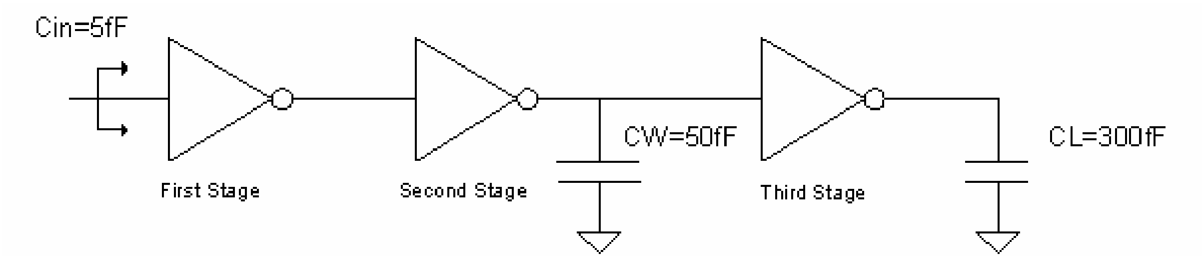

Figure 4b. Buffer Chain with Interstage Wire Capacitance