

# UNIVERSITY OF CALIFORNIA

## College of Engineering

### Department of Electrical Engineering and Computer Sciences

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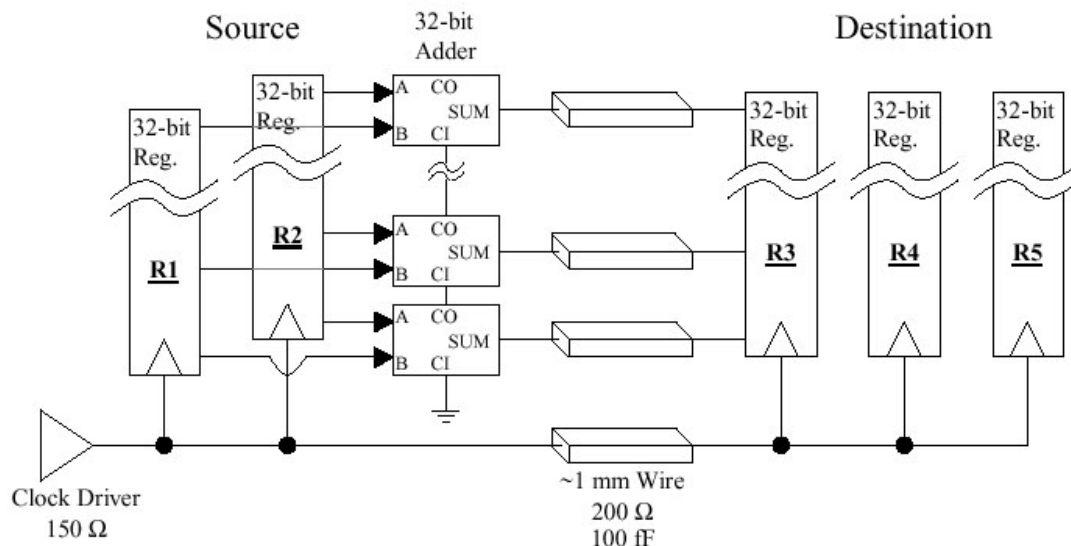
Homework #8

EECS 141

### Problem 1 – Timing & Race Conditions

The following circuit consists of a source portion, which adds the outputs of two registers R1 & R2 and a destination portion, which stores the sum in R3. The connections between the source and the destination are made by an automatic router, which creates wires with an average length of 1mm and containing an average of 10 vias in series. This leads to a resistance of about 200  $\Omega$  and capacitance of about 100 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3 and two other registers (R4 & R5) which happen to be close by. Each register presents a load of 300 fF to the clock driver.



Assume the following timing values for the logic:  $t_{\text{carry}} = 250$  ps,  $t_{\text{sum}} = 300$  ps (including the wire load),  $t_{\text{setup}} = 150$  ps,  $t_{\text{hold}} = 100$  ps,  $t_{\text{clk-Q}} = 50$  ps.

- Does this circuit have a race problem? What is the minimum clock period?
- What if you removed R4 and R5? Would there be a race problem? What would the new minimum clock period be?

- c) What if the driver were placed at the destination (with R3,R4 & R5)? Would there be a race problem? What would the new minimum clock period be?

**Problem2- Static Registers, Sizing, and Timing**

For a particular instance of the register shown in Figure 2, the source driver for input D is an inverter. Assume the cross-coupled inverters are all minimum-sized ( $W_p=2W_n$ ), 0.25um technology, and  $V_{dd}=2.5V$ . (Ignore Body effect)

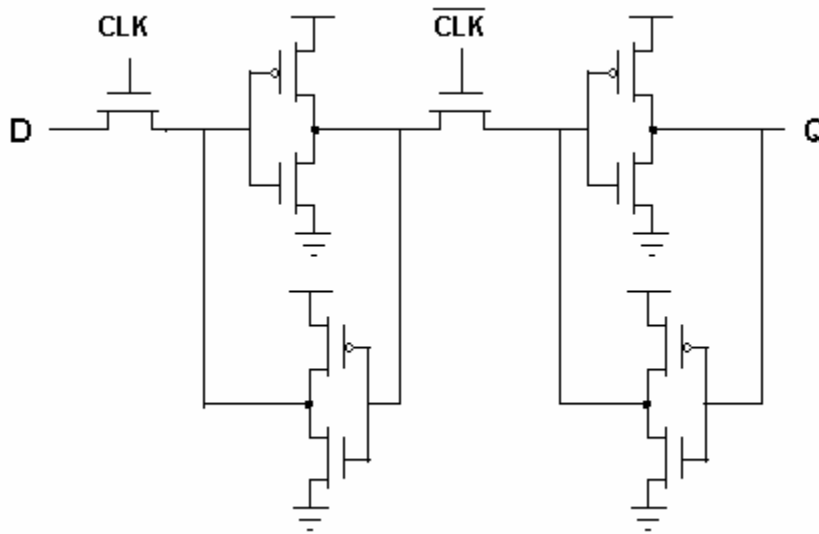
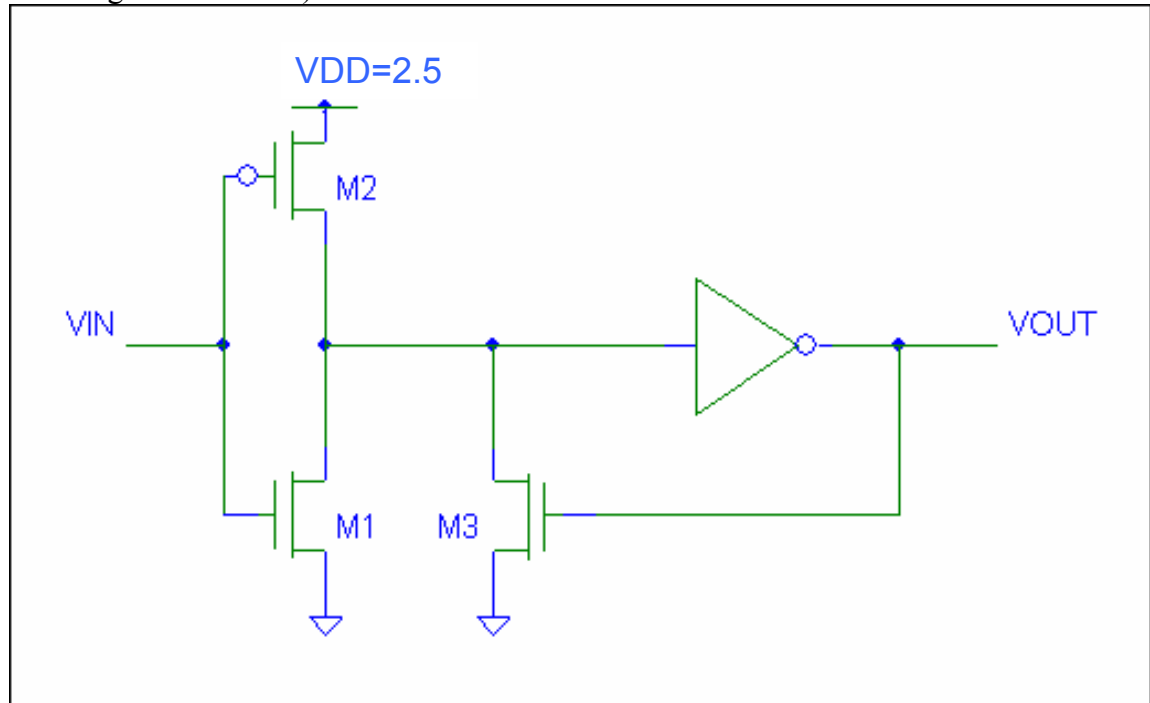


Fig. Static register.

- Find a sizing constraint on the source inverter and transmission gate that ensures proper functionality for storing a “0” (ignore body effect).
- How might you redesign the register to relax the sizing requirement on the driving stage?
- Given that the delay through the transmission gate is  $t_{TX}$ , and the delay through each of the inverters is  $t_{INV}$ , find expressions for the set-up time  $t_{SU}$ , propagation delay  $t_{CLK-Q}$ , and hold time  $t_H$  for this register.
- Using the sizing you derived in part (a), simulate the register and its source inverter in HSPICE. Determine the set-up time by adjusting the arrival times of D and the sampling edge of the CLK. Plot waveforms showing correct operation, and failure once the set-up requirement is violated.

### Problem3 – Schmitt Trigger

Consider the circuit below. The inverter is ideal, with  $V_M=V_{DD}/2$  and infinite slope. The transistors have  $|V_T|=0.4V$ ,  $k_n=115 \mu A/V^2$  and  $k_p=30 \mu A/V^2$ . M1 has  $(W/L)_1=1$ . Ignore all other parasitic effects in the transistors (velocity saturation, short channel length modulation).



- As  $V_{IN}$  goes from 0 to  $V_{DD}$  and back to 0 explain the sequence of events which makes this circuit operate as a Schmitt Trigger.
- Find the value of  $(W/L)_2$  such that when  $V_{IN}$  increases from 0 to  $V_{DD}$  the output will switch at  $V_{IN}=1.5V$ .
- Find the value of  $(W/L)_3$  such that when  $V_{IN}$  decreases from  $V_{DD}$  to 0 the output will switch at  $V_{IN}=1V$ .

### Problem 4 – Edge Triggered Register

Consider the following edge-triggered register. Assume that the clock inputs  $CLK$  and  $\overline{CLK}$  have a 0V to  $V_{DD}$  swing. Also assume (for parts a – c) that there is no skew between  $CLK$  and  $\overline{CLK}$  (i.e., the inverter delay to derive  $\overline{CLK}$  from  $CLK$  is zero). Assume that the rise/fall times on all signals are zero.

a) What type of register is this? Explain. (Positive Edge-Triggered Register or Negative Edge-Triggered Register).

b) What is the function of transistor M5-M8 and M13-M16?

c) Assume that the propagation delay of each clocked inverter (e.g., M<sub>1</sub>-M<sub>4</sub>) is  $T_{CK-INV}$  and the delay of inverters I<sub>1</sub> and I<sub>2</sub> is  $T_{INV}$ . Derive the expression for the set-up time ( $t_{SU}$ ), the propagation delay ( $t_{c-q}$ ) and the hold time ( $t_h$ ) in terms of the above parameters,  $T_{CK-INV}$  and  $T_{INV}$ . Explain your results.

