

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
Last modified on September 12, 2004 by Henry Jen and Stanley Wang (henryjen@eecs.berkeley.edu)

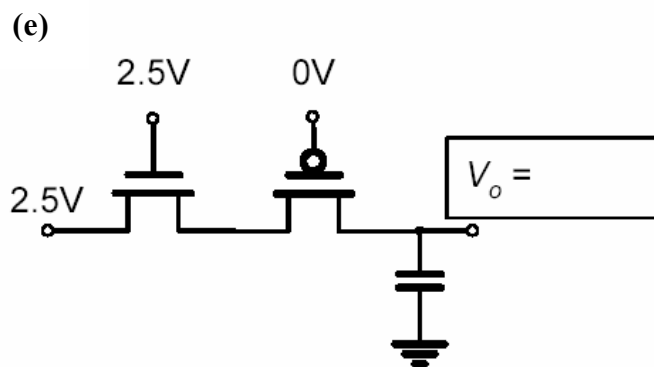
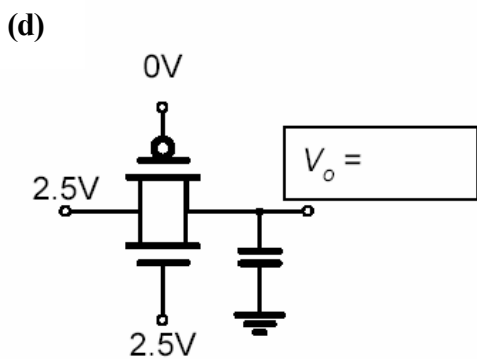
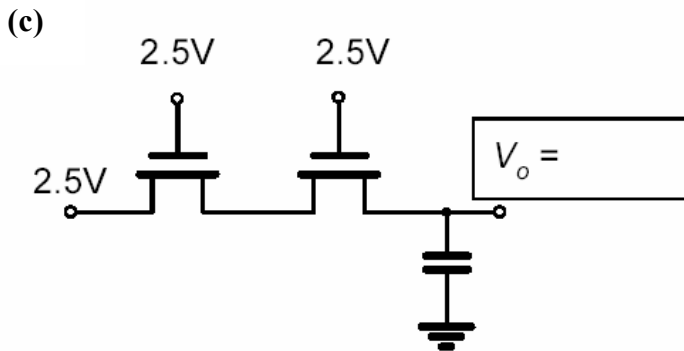
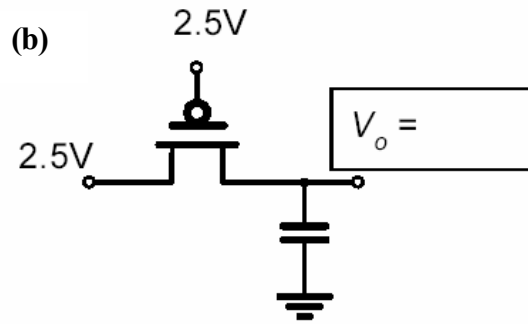
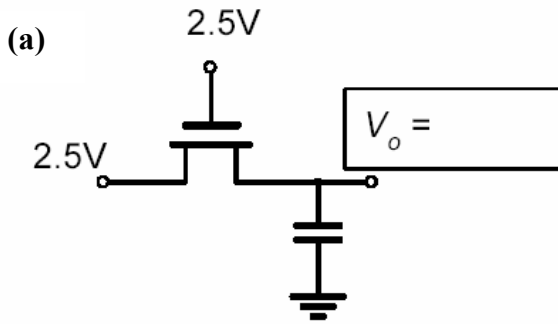
Borivoje Nikolic

Homework #3
 Due Thursday, September 23rd

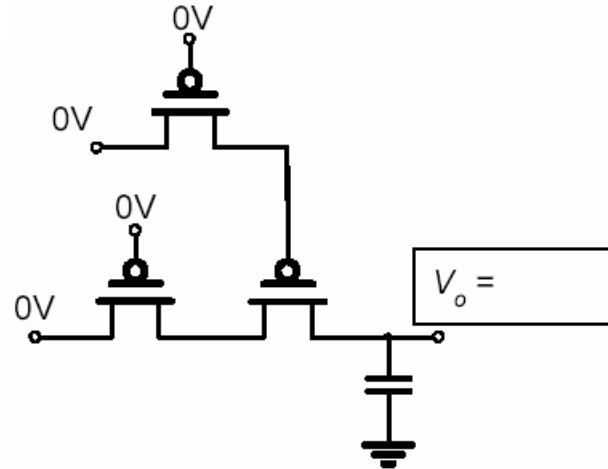
EECS 141

Problem #1

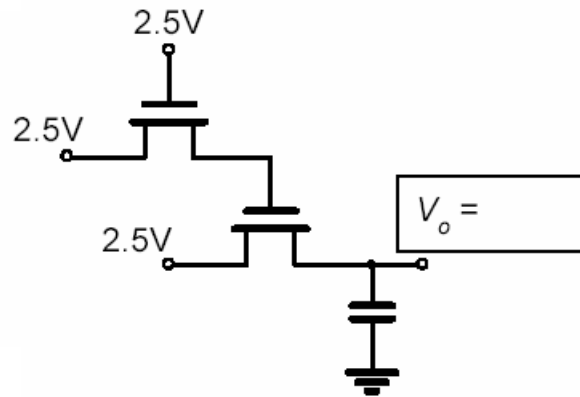
Find the final value of the voltage V_o . Assume $V_{TN}=|V_{TP}|=0.6V$. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.



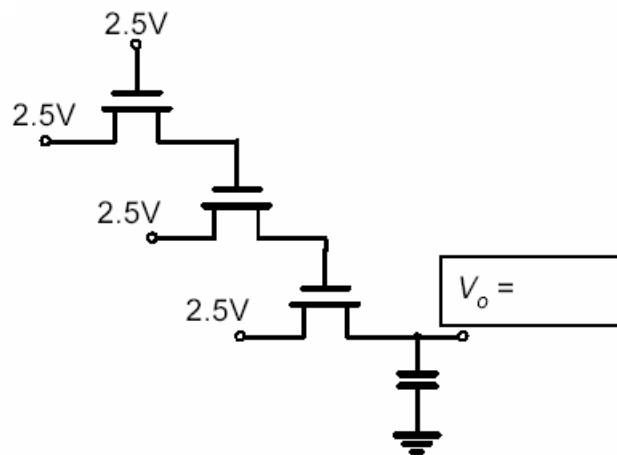
(f)



(g)



(h)



Problem #2

Consider the inverter circuit shown in Figure 2 with an ideal square-wave input. Assume that short-channel effects are negligible— meaning $V_{DSAT} \gg V_{DS}$, $V_{GS} - V_T$.

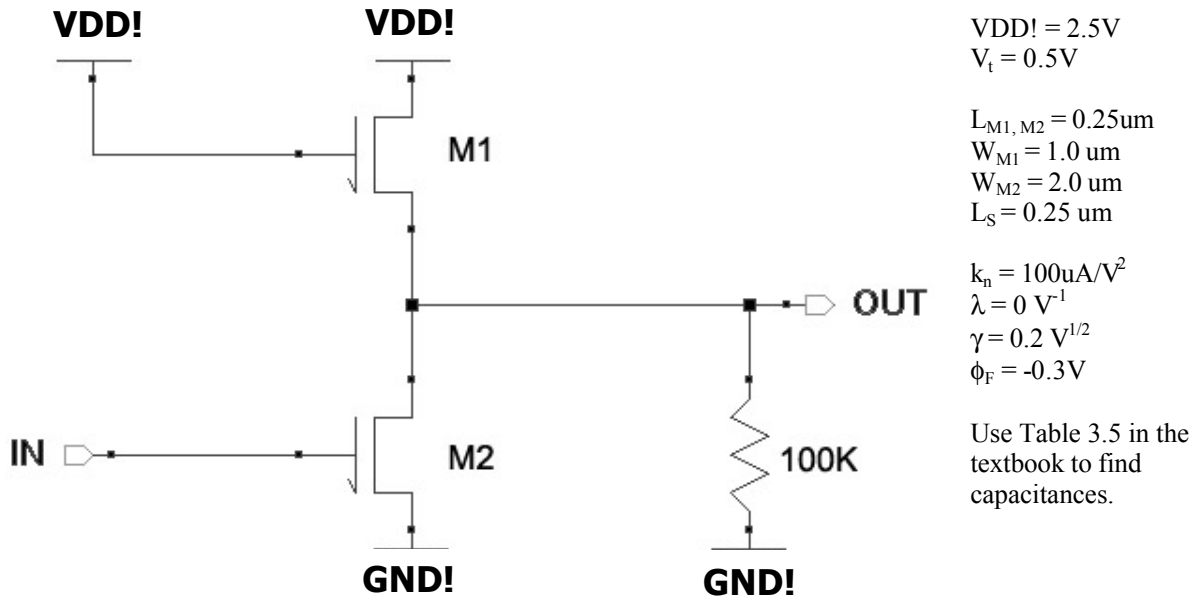


Figure 2

Note: A node name followed by a “!” (i.e. $V_{DD!}$ and $GND!$) denotes a global node in a netlist.

Using the information above and references in the text, determine the following:

- Find V_{OH} and V_{OL} . Hint: Both the load and driver transistors are NMOS, so don't say 2.5V and 0V!
- Calculate t_{pLH} and t_{pHL} . This will require you to find a R_{eq} and C_{eq} in each case. There's no explicit load so we'll consider the self loading (only internal capacitances) that is seen at the output (there should be two components).
- Assuming a normal pmos/nmos inverter is the load presented at the output, what other capacitances would we have to account for in the C_{eq} calculation in addition to those you used for part b)?
- Find the static power dissipation for:
 - $V_{in} = 0.0V$
 - $V_{in} = 2.5V$

Problem #3

- a) It is always good to get a feel for design rules in a layout editor. Fire up Cadence with the 0.25um technology file used in the lab session. Place a minimum sized NMOS transistor and examine the dimensions. The layers are listed and shown below in Figure 3a. Determine and list the following:
- Minimum Transistor Length
 - Minimum Transistor Width
 - Minimum Source/Drain Area
 - Minimum Source/Drain Perimeter

Please list the design rules you come across that lead to your results.

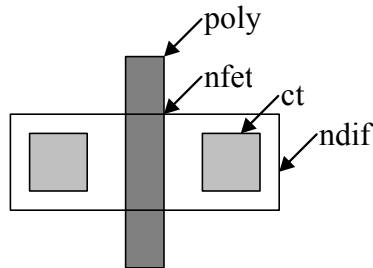


Figure 3a

n

- b) We desire a minimum sized CMOS inverter with a symmetrical VTC ($V_M = V_{DD}/2$) in the 0.25um technology. Calculate the following for the pull-up PMOS transistor in the design.
- Minimum Transistor Length
 - Minimum Transistor Width
 - Minimum Source/Drain Area
 - Minimum Source/Drain Perimeter

Assume the following:

$V_{DD} = 2.5V$, $V_M = 1.25V$, and refer to Table 3.2 in the textbook.

- c) Using the same minimum size inverter from part b), determine the input capacitance (i.e. the load it presents when driven). Please calculate the capacitance during a transition. From these, determine the total load capacitance that the inverter presents.
**Hint: Consider the Miller effect*
- d) Using the g25 model provided in '[~ee141/MODELS/g25.mod](#)', please verify the accuracy of your results in part c by determining the total input capacitance in a high-low and a low-high transition with HSPICE and comparing with your total capacitance in part c. Turn in your HSPICE input deck.

You'll notice there are five corners, TT, FF, SS, FS, and SF. These represent the different variation extremes we can expect due to process variations. For example, TT stands for NMOS: typical, PMOS: typical. FS stands for NMOS: fast, PMOS: slow etc. For this homework, please use the TT model.

To use these models, include the following in your HSPICE deck:

.lib '~ee141/MODELS/g25.mod' TT

- e) Determine V_{IH} , V_{IL} , NM_H , and NM_L .
**Hint: Refer to Eq's 5.3 and 5.10 in the textbook for r and g*

Problem #4

- a) Figure 4a depicts the $I_d - V_{OUT}$ curve of a typical NMOS transistor
 Figure 4b depicts the $I_d - V_{OUT}$ curve of a typical PMOS transistor

Assume we use these FETs to create a CMOS inverter. Using this family of curves, graph the VTC, and calculate V_M , V_{IL} , and V_{IH} .

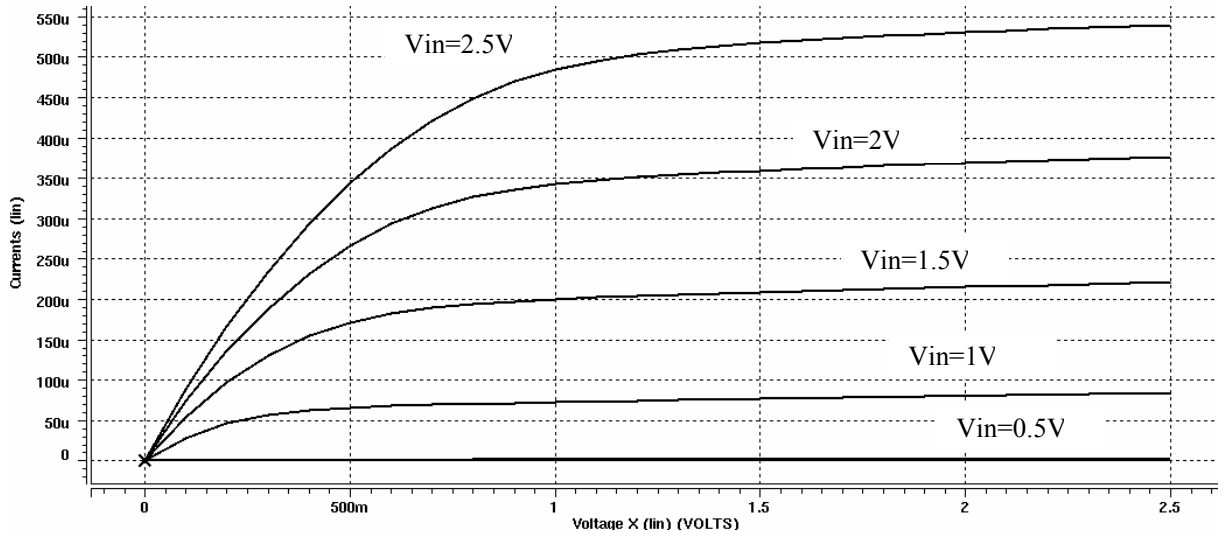


Figure 4a

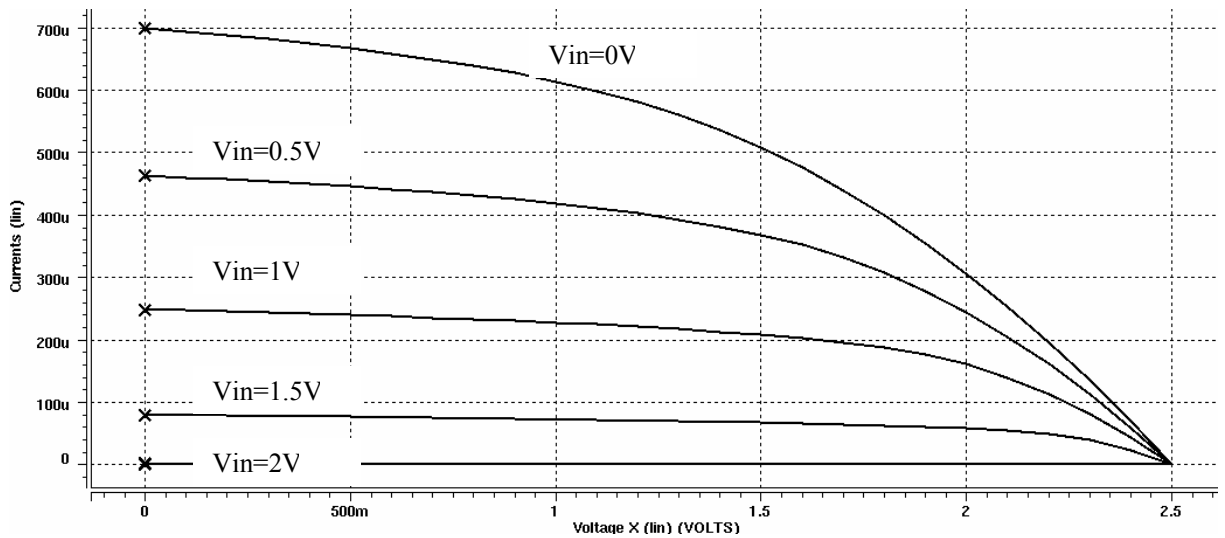


Figure 4b

- b) The curves above were generated using the TT corner in Hspice. Intuitively explain how using the FS and SF corners will affect the above $I - V$ curves and the VTC.