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Homework #5: Delay

EECS 141

Problem #1 Gate Delay

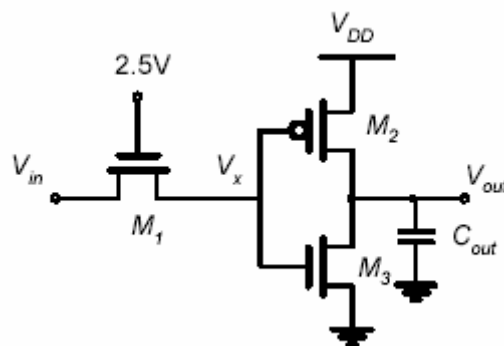
Consider a three-transistor circuit as shown in the figure below. $V_{DD} = 2.5V$ and input signal switches between 0 and V_{DD} with sharp rise and fall times. Use the transistor parameters below. Ignore body effect. All transistors are minimum length, $L = 0.25 \mu m$. Transistor widths: $W_2 = 2 \mu m$, $W_1 = 1 \mu m$.

NMOS:

$$V_{Tn} = 0.4, k'_n = 115 \text{ uA/V}^2, V_{DSAT} = 0.6V, \lambda = 0, \gamma = 0.4 \text{ V}^{1/2}, 2\phi_f = -0.6V$$

PMOS:

$$V_{Tp} = -0.4V, k'_p = -30 \text{ uA/V}^2, V_{DSAT} = -1V, \lambda = 0, \gamma = -0.4 \text{ V}^{1/2}, 2\phi_f = 0.6V$$



- a) Find the M_3 transistor width such that the switching point of the inverter (V_M) is placed in the middle of the V_x signal swing.
- b) Find the t_{pLH} delay of this circuit. $C_{ox} = 6\text{fF}/\mu\text{m}^2$. Overlap capacitances are $C_o = 0.3 \text{ fF}/\mu\text{m}$. Bottom-plate PN junction capacitances are $2\text{fF}/\mu\text{m}$ of device width. Ignore the sidewall capacitances. Ignore the impact of rise/fall times on propagation delay. $C_{out} = 10\text{fF}$.

Problem #2 Elmore Delay

Consider the circuit of Fig. 2a. The size of the transistors is indicated as r ($r=1$ means minimum size; $r=2$ means $W=2 \times W_{\min}$, etc.). Assume all nodes (except V_{In}) are initially at $0V$. A voltage waveform ϕ , shown in Fig. 2b is applied to the circuit.

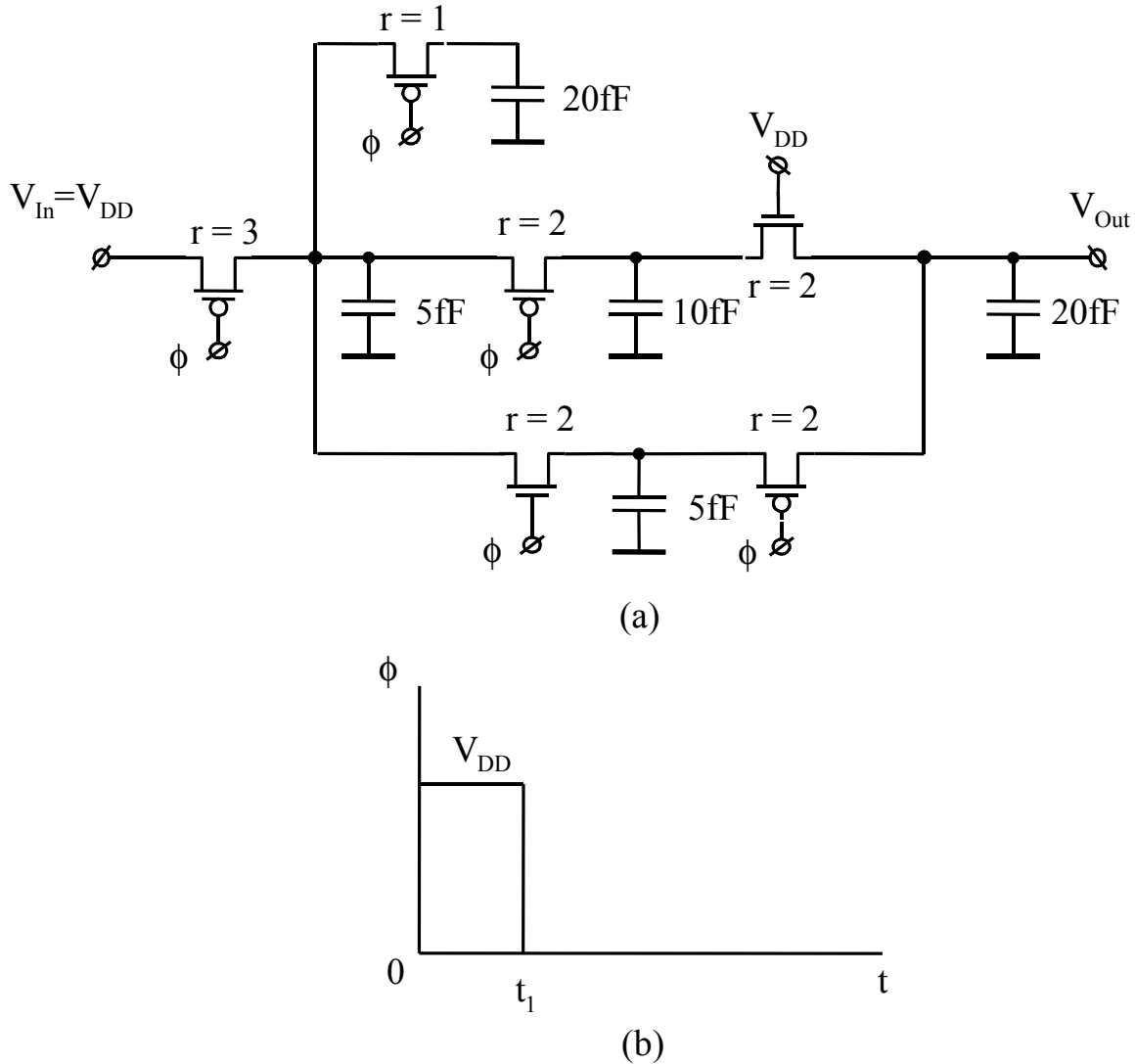


Figure 2

We will use an equivalent resistor-capacitor model to find the propagation delay of the circuit. Assume the following parameters for the minimum-size transistors: $R_{eqN}=10k\Omega$ (NMOS), $R_{eqP}=20k\Omega$ (PMOS), $C_{gs}=C_{gd}=0.5fF$; $C_{db}=C_{sb}=1fF$. Ignore overlap capacitors and feedthrough from the gates of the switching transistors to the circuit nodes.

- Draw the equivalent R-C circuit after $t=t_1$ including all relevant resistors and capacitors and indicate their values.
- From the equivalent model calculate the delay between $t=t_1$ and the time when $V_{out}=V_{DD}/2$ (Assume V_{DD} is larger than several V_T).

Problem #3 Inverter Sizing and Wire Delay

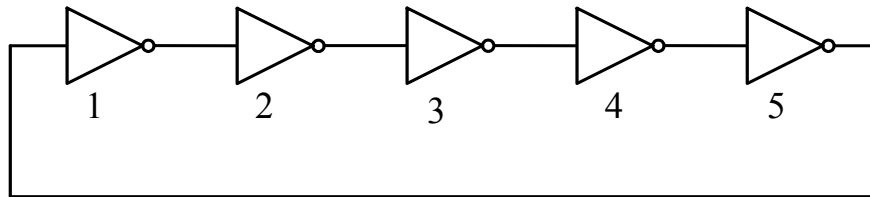


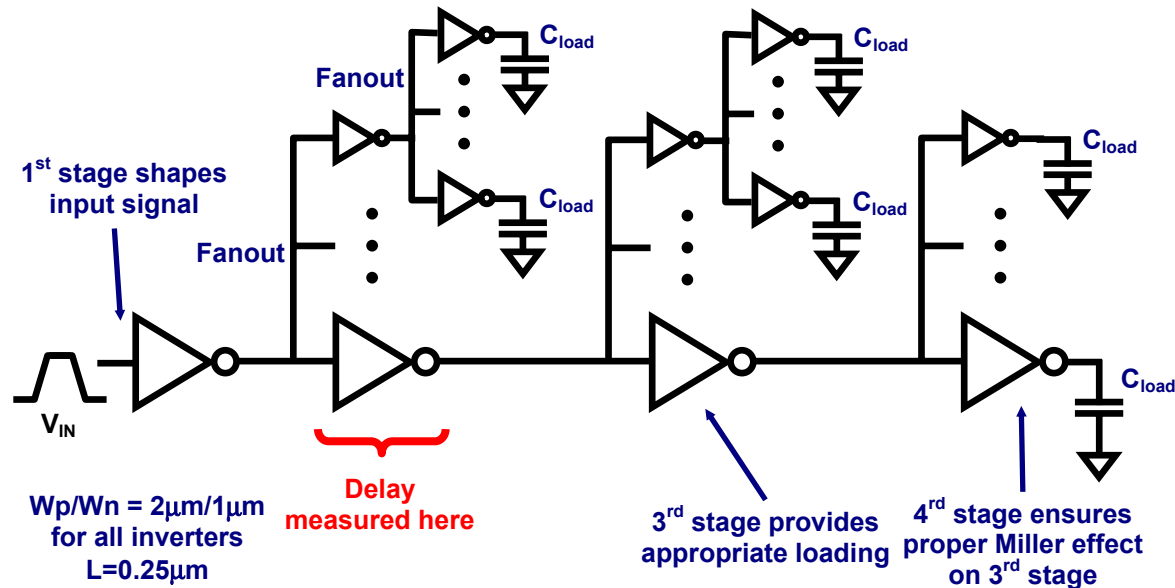
Figure 3

Figure 3 shows a ring oscillator. This circuit is used for evaluating the gate delay in a certain technology (see pp. 28-29). We will use it in a slightly different way. Assume the intrinsic propagation delay of a minimum-size inverter is 15ps. Also assume the input capacitance is $C_g=4\text{fF}$ and $\gamma=2$ (see Eq. 5.29).

- a) Calculate the frequency of oscillation of the ring oscillator built with minimum-size inverters.
- b) Now suppose that inverter 5 is connected to inverter 1 with a metal-1 wire of width $1\ \mu\text{m}$ and length 1mm. The sheet resistance of aluminum in metal-1 is $0.08\Omega/\square$. Assume field oxide underneath the wire and no other wires in the vicinity. Using Table 4.2 in Chapter 4 find the new oscillation frequency of the ring oscillator.
- c) Keep inverter 1 at minimum size and size the other inverters to maximize the frequency of oscillation with the wire present. What is the maximized frequency?

Problem #4 Self-loaded Inverter Delay

You would like to find the self-loaded (i.e. no external capacitive load...just the internal capacitances) delay of an inverter fabricated in our not-so-technologically-advanced 2.5V 0.25 μm process. However, since you are an EE141 expert, you know that you cannot simply measure this delay in HSPICE with a single unloaded inverter due to problems with Miller multiplication and capacitive coupling. Luckily, you are also an HSPICE expert. So first, you set up a SPICE deck to simulate the following 4-stage inverter chain (with some fanout):



Using this circuit, you can get an accurate measurement of the real delay in a circuit by measuring the delay of the second inverter in the chain. With a reasonable input rise/fall time ($\sim 200\text{ps}$), the first inverter should do a good job of creating a realistic input signal to the second inverter. The third stage provides an appropriate load for the second inverter...because in real life, we would likely be driving some number of gates with an output signal. You put a fourth stage just for good measure...to make sure that the Miller effect for the third stage is reasonable. You also remember to put a reasonable load capacitance ($\sim 20\text{fF}$) at the output of these load inverter stages so that there is no spurious Miller effect going on. Of course, you don't forget the fanout of the load inverter stages either. Since there are so many inverters, you know that using the ".SUBCKT" command would make life really easy. You also remember that using the "m" tag (multiplicity parameter) when calling a subcircuit could be helpful.

In order to get the self-loaded delay, you decide to do the following:

- a) Use HSPICE to find the average propagation delay (average of low-high and high-low transitions) for an inverter in this process for a fanout of 1, 2, 3, and 4. Simply measured the delay of the second inverter in this chain. Use the SPICE model in '/home/ff/ee141/MODELS/g25.mod'. Plot the propagation delay as a function of the fanout.

- b) In your plot, the points should fall in a straight line...find the best-fit line through the data. This allows you to extrapolate the delay for a fanout of 0 (intercept with the x-axis). This is your self-loaded delay. What is this value?
- c) In your plot, the slope of the line tells you about the additional delay per fanout. What is this value?
- d) From your answers to b) and c), find the C_d/C_g , the ratio between the drain capacitance (self-load) and the gate capacitance (load per additional fanout). Assuming that $C_g=C_{ox}(W_n+W_p)L$, compute C_g and C_d .
- e) Using C_d (and C_g if you like), compute R_{eq} . Just use the average delay, ignoring differences between high-low and low-high transitions.