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Borivoje Nikolic Homework #6: CMOS logic

EECS 141

**Problem 1 – CMOS Gate Design and Implementation**

- a) Design  $F = \overline{BC + AC + AB}$  in combinational CMOS logic using the least number of devices. Draw the schematics and size the transistors with respect to unit width NMOS and PMOS devices so that worst case equivalent resistances are equal to those of a unit sized inverter ( $R_{unit}$ ). Assuming  $2k'_p = k'_n$ . Which input pattern(s) would give you the worst and best equivalent pull-up or pull-down resistance (identify 4 input patterns here).
- b) Draw the Logic Graphs corresponding to the circuit and identify the Euler paths
- c) Using the Euler paths you found draw the stick diagram for the implementation. You don't need to distinguish different widths in the stick diagram.

**Problem #2: CMOS Logic and Euler Paths**

For this problem we will use the following function:  $F = (a * b) \oplus [c * (d + e)]$ . (Note:  $\oplus$  stands for an XOR operation). All signals and their complements are available as inputs.

- a) Find a PDN configuration, which implements the function  $Y = A \oplus B$  with four transistors.
- b) Using the result from a), draw the CMOS logic circuit that implements the function F. Size it such that it has the same pull-up/pull-down strength as a minimum sized 2/1 inverter.
- c) Determine the order of the input signals, which allows the largest number of diffusions to be shared. Show the signal graphs used to arrive at your solution.

