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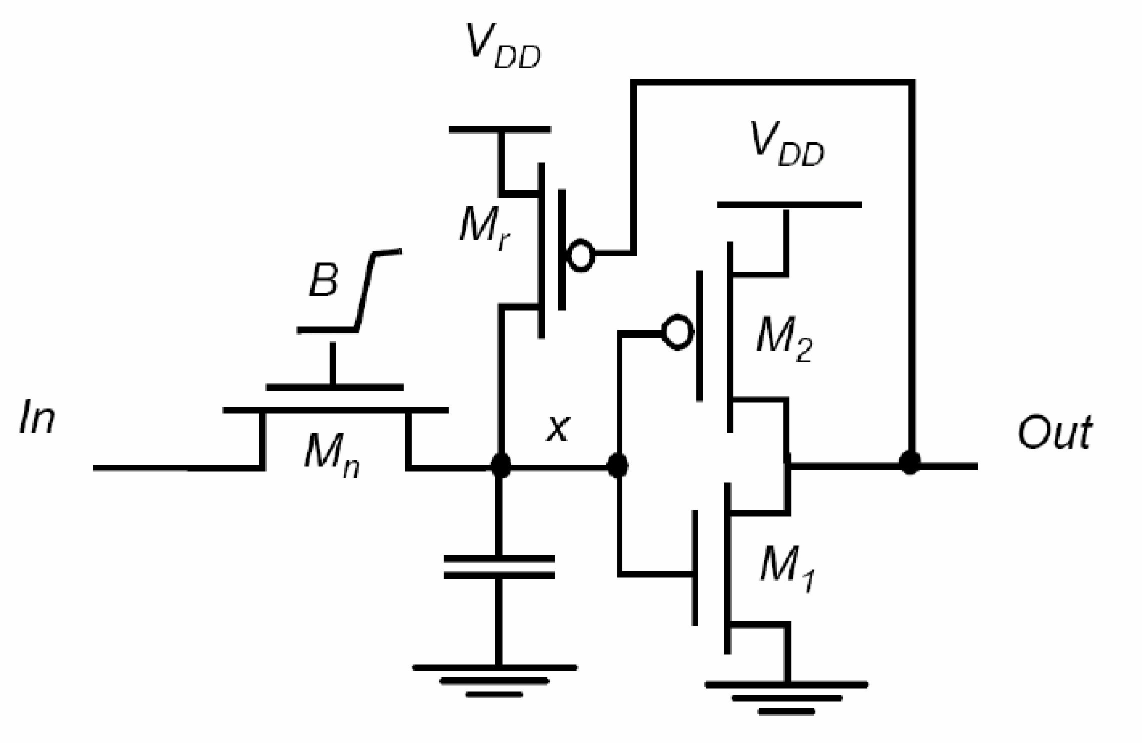
Borivoje Nikolic   Homework #7: CMOS Logic and Logical Effort   EECS 141

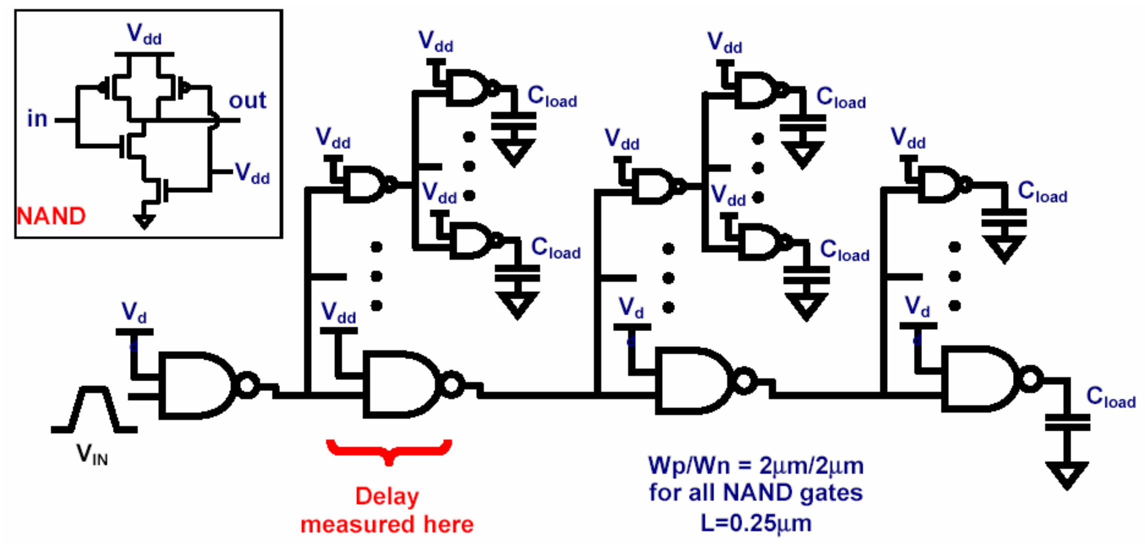
<u>Problem #1 Pass transistor gate with level restorer</u>



Consider the circuit above. Let C_x = 50fF. M_r has W/L = 0.5/0.5, M_n has W/L=0.5/0.25. Assume the output inverter doesn't switch until its input equals $V_{DD}/2$.

a) What is the function of M_r?
b) Describe qualitatively how this circuit operates for H→L and L→H input transitions.
c) How long will it take M_n to pull node x down from 2.5V to 1.25V if V_{In} is set to 0V and B is at 2.5V?
d) How long will it take M_n to pull node x up from 0 to 1.25V if V_{In} is 2.5V and B is at 2.5V?
e) What is the minimum value of V_B necessary to pull V_x down to 1.25V when V_{In}=0?
f) If node B is at 2.5V, what is the maximum size of M_r such that the circuit still operates as intended?

Problem #2 – Self-loaded NAND Delay



a) Use HSPICE to find the average propagation delay for a NAND gate in this process for a fanout of 1, 2, 3, and 4. Plot the propagation delay as a function of the fanout.

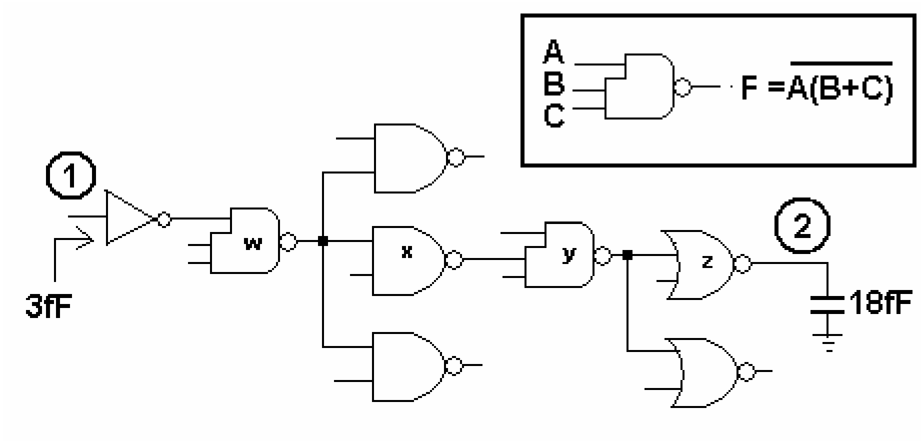
b) What is the self-loaded delay of a NAND gate?

c) What is the slope of the best-fit line through your data points (additional delay per fanout)? This slope is related to the number obtained from logical effort calculations when you divide by the slope for an inverter (HW5 problem 4)…compare $slope_{NAND}/slope_{INV}$ to the theoretical value from logical effort.

d) From your answers to b) and c), find the C_d/C_g. Compute C_g and C_d.

e) Compute R_{eq}.

Problem #3 – Logic and Logical Effort



a) A three-input XNORT gate (see insert above) works like a two-input NOR as long as input A is high; otherwise, the output is stuck high. Implement the XNORT gate in complementary CMOS, and size all transistors such that the worst-case delay is equal to that of a minimum sized 2/1 inverter. Find the logical effort associated with each input.

b) Assuming all input combinations are equally likely, what is the transition activity (probability) of a XNORT gate? Averaged over many cycles, will a XNORT gate typically consume more or less power than a two-input NOR gate, if they both drive equally large output loads? What about a two-input XOR?

c) For the logic path from node (1) to node (2) shown in the figure above, find the path branching effort, path electrical effort, path logical effort, and total path effort. What is the optimum effort per stage for minimizing delay?

d) Find the input capacitances {w, x, y, z} necessary for each of the gates in the path in order to achieve the optimum effort per stage.