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Homework #10

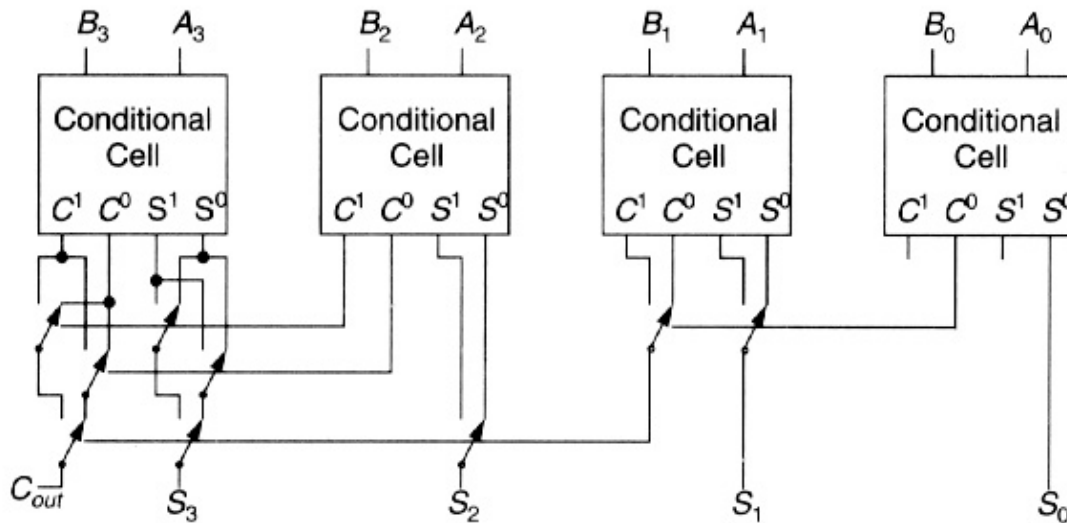
EECS 141

**Problem 1 - An introductory adder problem**

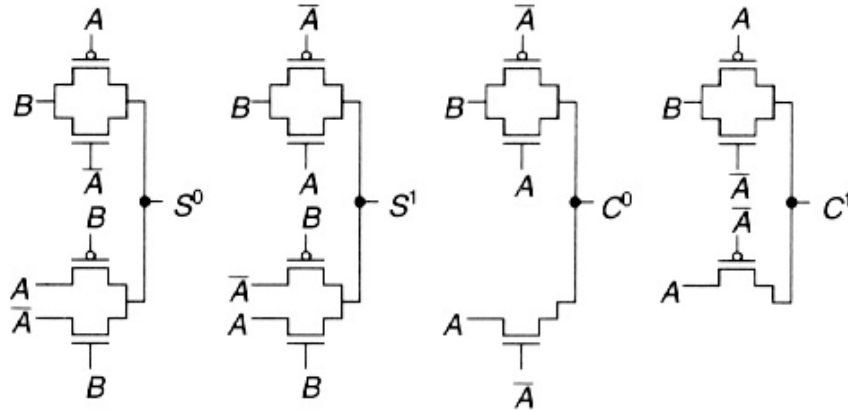
- a) Show that the expression for  $S$  in Eq. 11.6 is equivalent to the one in Eq. 11.1
- b) Convince yourself that the circuit in Fig. 11.4 implements Eq. 11.6. Size the transistors such that each stage (carry and sum) has the same pull-up/pull-down strength as a minimum-sized 2/1 inverter. Find the logical effort for each input (consider the carry and sum stages separately).
- c) Now consider the mirror adder in Fig. 11.6. Make sure that you understand what it does. Size the transistors such that each stage (carry and sum) has the same pull-up/pull-down strength as a minimum-sized 2/1 inverter. Find the logical effort for each input (consider the carry and sum stages separately). How does it compare to the architecture in Fig. 11.4?

**Problem 2 – Conditional Sum Adder**

Here is a neat adder structure called the conditional sum adder. Shown below is a 4-bit version of the circuit. Note that in the diagram, multiplexors are represented by switch-controlled arrows.



Using a pass-transistor implementation, the circuit schematic for each adder cell can be:

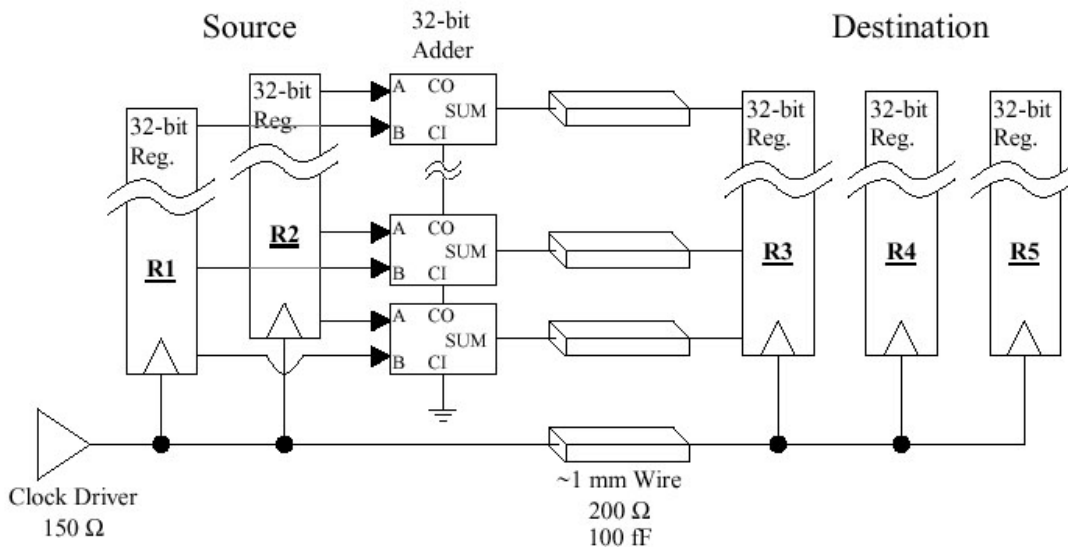


- Derive Boolean equations for the four outputs of the one-bit conditional adder cell
- Based on your results to part a), describe how the 4-bit adder works.
- Derive an expression for the propagation delay of the adder as a function of the number of Bits,  $N$ . Assume that the delay through each conditional cell is  $t_{\text{cell}}$  and that the delay of a MUX is  $t_{\text{MUX}}$ .

### Problem 3 – Timing & Race Conditions

The following circuit consists of a source portion, which adds the outputs of two registers R1 & R2 and a destination portion, which stores the sum in R3. The connections between the source and the destination are made by an automatic router, which creates wires with an average length of 1mm and containing an average of 10 contact holes in series. This leads to a resistance of about 200  $\Omega$  and capacitance of about 100 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3 and two other registers (R4 & R5) which happen to be close by. Each register presents a load of 300 fF to the clock driver.



Assume the following timing values for the logic:  $t_{\text{carry}} = 250$  ps,  $t_{\text{sum}} = 300$  ps (including the wire load),  $t_{\text{setup}} = 150$  ps,  $t_{\text{hold}} = 100$  ps,  $t_{\text{clk-Q}} = 50$  ps.

- Does this circuit have a race problem? What is the minimum clock period?
- What if you removed R4 and R5? Would there be a race problem? What would the new minimum clock period be?
- What if the driver were placed at the destination (with R3, R4 & R5)? Would there be a race problem? What would the new minimum clock period be?

#### **Problem 4 – DRAM Memory Cell**

A 1-T DRAM cell as following consists of a single transistor connected in series with a capacitor. For a read, the bit line is precharged to  $V_{DD}/2$  by a clocked precharge circuit. Then, the access transistor is turned on by applying  $V_{DD}$  to the word line. A write is performed by applying  $V_{DD}$  or  $GND$  to the bit line and  $V_{DD}$  to the word line. Assume that  $V_{T0} = 0.4 \text{ V}$ ,  $\gamma = 0.3 \text{ V}^{1/2}$ ,  $|2\phi_F| = 0.6 \text{ V}$

- Find the maximum voltage across the storage capacitor  $C_s$  after writing a 1 into the memory cell (i.e., bit line is driven to  $V_{DD} = 2.5 \text{ V}$ ).
- Ignoring leakage currents, find the voltage on the bit line when this “1” is read from the memory cell.

