

Problem #1 Logical Effort of Transmission Gates

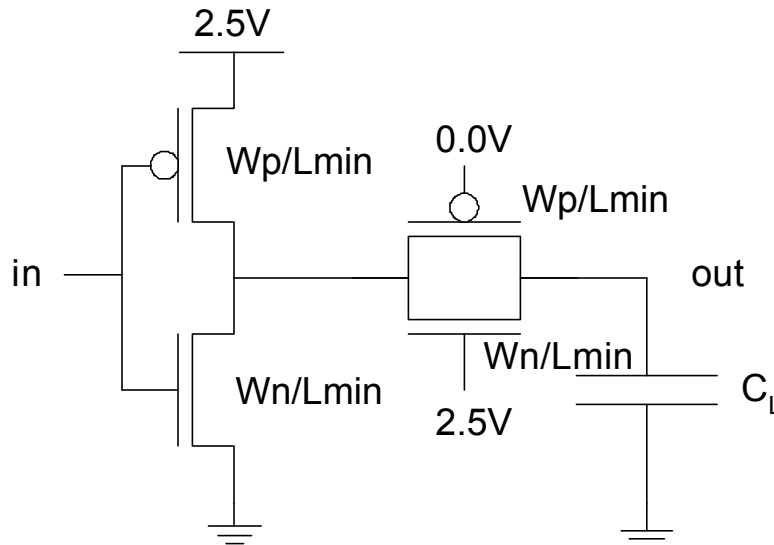


Figure 1

Calculate the logical effort of the circuit shown in Figure 1 given that $W_p=2W_n=2W_{min}$.

Problem #2 Domino logic

Suppose we want to implement two logic functions given by $F=A+B+C$ and $G=A+B+C+D$. Assume both true and complementary signals are available.

- a) Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.
- b) Discuss any conditions under which this implementation would fail to operate properly.
- c) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b)?

Problem #3 Charge sharing

- a) Assuming that all inputs of the circuit shown in Figure 3 below are initially 0 during the precharge phase and that all internal nodes are at 0V, calculate the voltage drop on V_o , if A changes to 1 ($V_{DD}=2.5V$) during the evaluate phase. It is given that $V_{tn0}=0.5V$, $2f_F=0.6V$ and $\gamma=0.4V^{0.5}$.
Hint: Don't forget the body effect.

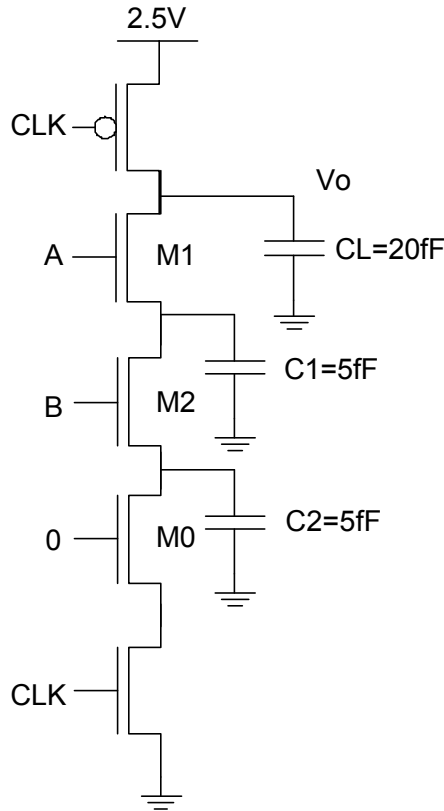


Figure 3

- b) Now calculate the voltage drop on V_o if both A and B change to 1 (under the above conditions).
c) What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M0) if the output should not fall below 0.9V during the evaluate phase? Assume that each one of the new transistors has the same intrinsic capacitance (to ground) as M1 and M2 ($C=5fF$).