

**Problem 1 – Static Registers, Sizing, and Timing**

For a particular instance of the register shown in Figure 1, the source driver for input D is an inverter. Assume the cross-coupled inverters are all minimum-sized ( $W_p=2W_n$ ),

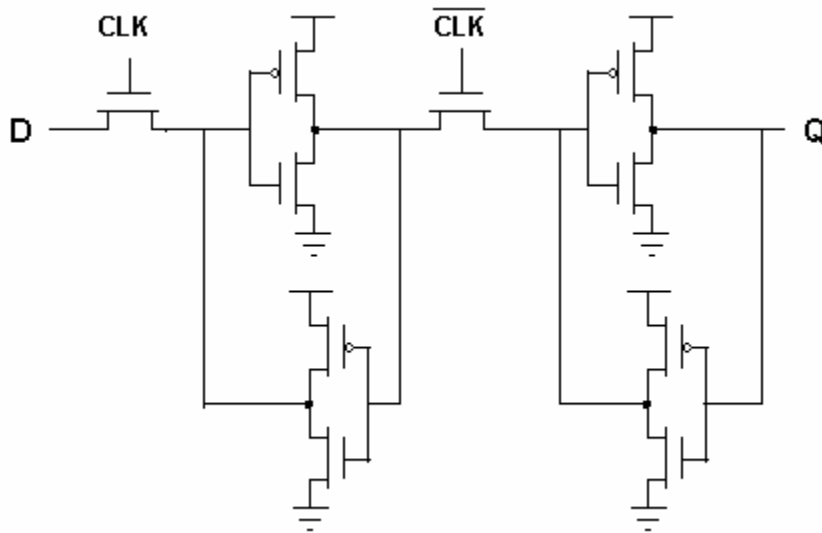
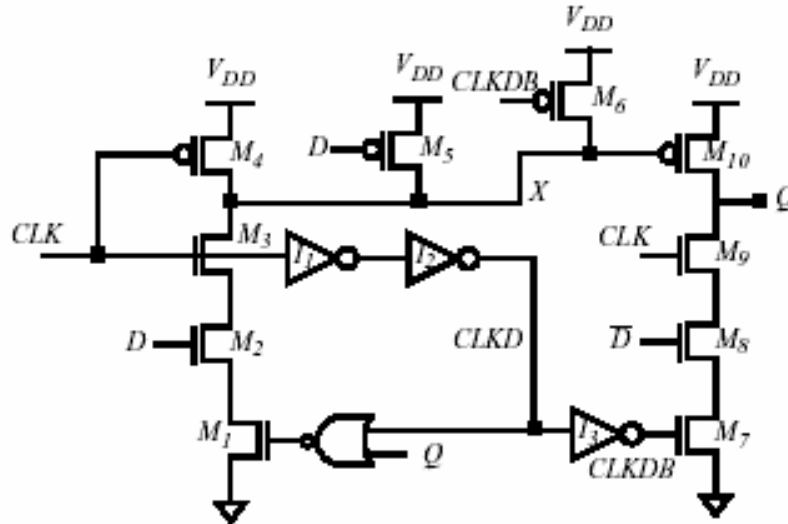


Figure 1. Static register.

- a. Find a sizing constraint on the source inverter and transmission gate that ensures proper functionality for storing a “0” (ignore body effect) (Hint: size the pull-down of the driving inverter the same as the pass-transistor gate).
- b. How might you redesign the register to relax the sizing requirement on the driving stage?
- c. Given that the delay through the transmission gate is  $t_{TX}$ , and the delay through each of the inverters is  $t_{NV}$ , find expressions for the set-up time  $t_{SU}$ , propagation delay  $t_{CLK-Q}$ , and hold time  $t_H$  for this register.

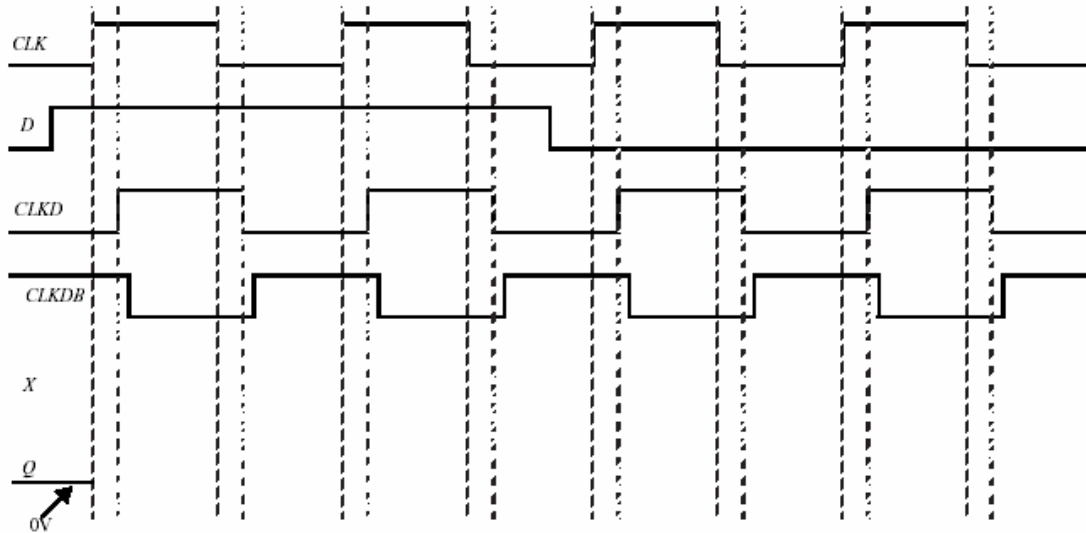
### Problem 2 – Sequential Circuit

Consider the following sequential circuit. Assume that there is no delay between  $D$  and  $\overline{D}$  (i.e., the inverter delay to obtain  $\overline{D}$  from  $D$  is 0). Assume that the output is statically held using circuits not shown here (i.e., ignore leakage effects for this problem). Assume that the rise/fall times on all signals are zero.



a) Complete the following timing diagram for  $X$  and  $Q$ .

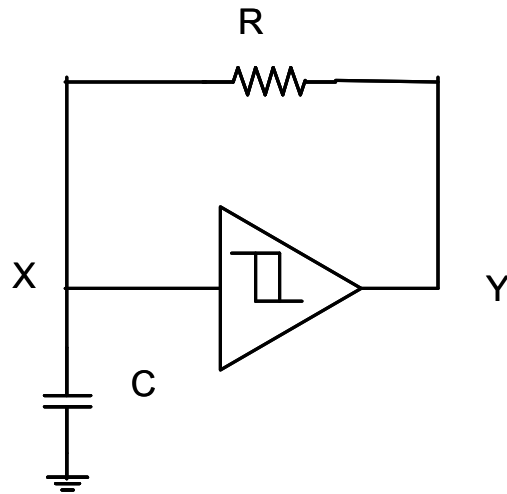
Assume that the inverter delay is much smaller than the clock period and that appropriate set-up/hold times are met. Assume that each gate ( $I_1$ ,  $I_2$ ,  $I_3$ , NOR,  $M1$ - $M4$  and  $M7$ - $M10$ ) takes 1 time unit for a low to high or high to low transition. Also assume that it takes 1 time unit to charge node  $X$  through  $M5$  or  $M6$ . Both the propagation and contamination (i.e., minimum) delay are equal to 1.



b) What is the set-up time for this circuit if glitches on the output  $Q$  are acceptable? Explain.

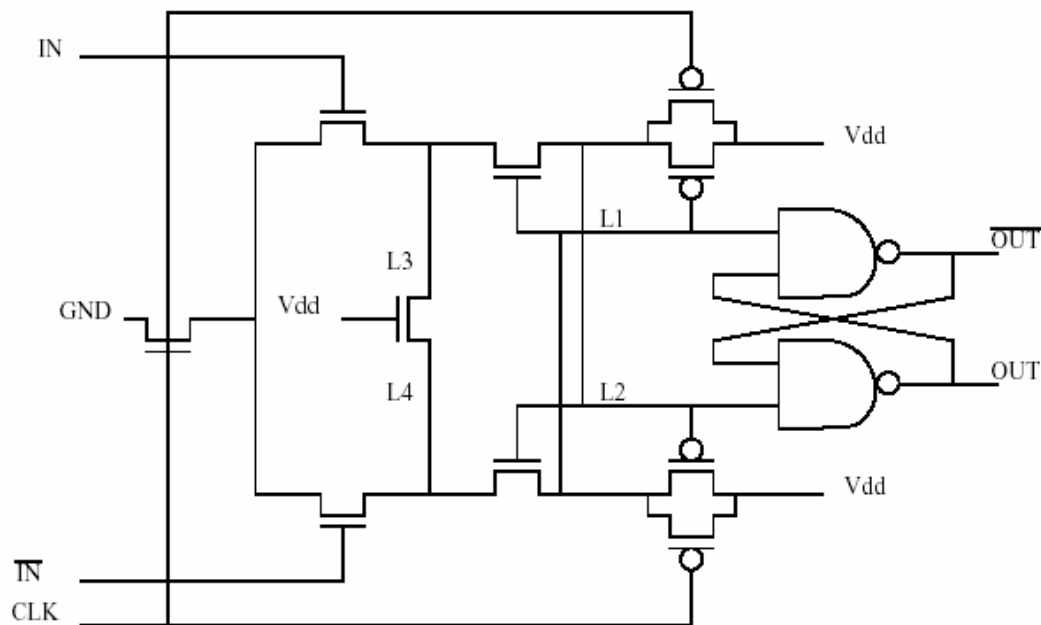
### Problem 3 -- Multi-Vibrator

[M, None, 7.6] The circuit in Figure 8 operates at a supply voltage  $V_{dd}$  of 2.4V and uses Schmitt triggers with the following threshold voltages:  $V_{M+} = 1.6V$ ,  $V_{M-} = 0.8V$ .



- Identify whether the circuit is monostable, bistable, or astable?
- Draw the waveforms at nodes X, Y. Mark all important voltage levels.
- Calculate the key timing parameter for this circuit (propagation delay for bistable, pulse width for monostable, and time period for astable) in terms of R and C. You can assume that gate delays are negligible compared to the delay of the RC network.

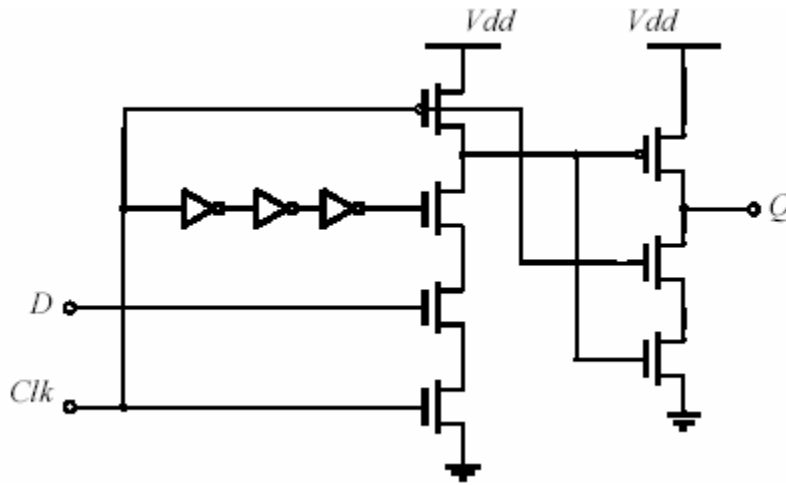
#### Problem 4 -- Low Power Edge-Triggered Register



The flip-flop shown in the above figure is used in the StrongARM microprocessor developed by Digital Equipment Corporation for the Portable Electronic Device (PED) market. Note that it is fully differential. The following questions will help you understand the operation of this flip-flop. No calculations are necessary for this problem.

- When clock is low is the flop holding or is it transparent? Why? (2 sentences)
- What is the purpose of the shorting transistor connecting nodes L3, L4? (2 sentences)
- What is the main advantage of this flip-flop from a low power perspective? (1 sentence)
- What determines the setup time for this flip-flop? Draw a timing diagram showing the timing relationship between the data and the clock. (1 sentence)

### Problem 5 -- Sequential circuits



- Would the sequential circuit from the figure above be considered a latch, a master-slave latch pair or a pulse-triggered latch? Briefly explain your answer.
- All transistors in this circuit are unit-sized, with equivalent resistances  $R$  and gate capacitances  $C$  (ignore diffusion capacitances). Calculate the propagation delay  $t_{Clk-Q}$  for high-to-low and low-to-high transitions. Load on the output  $Q$  is equal  $12C$ . Ignore the signal slopes in delay calculation.
- This circuit does not strictly follow the rules for designing sequential logic discussed in the class. List three major problems in the operation of this circuit.