

1. SRAM bitline design

In this phase, you will assemble (in both schematic and layout) a bitline consisting of 64 SRAM cells designed in phase I of the project, together with peripheral circuitry as shown in Figure 1.

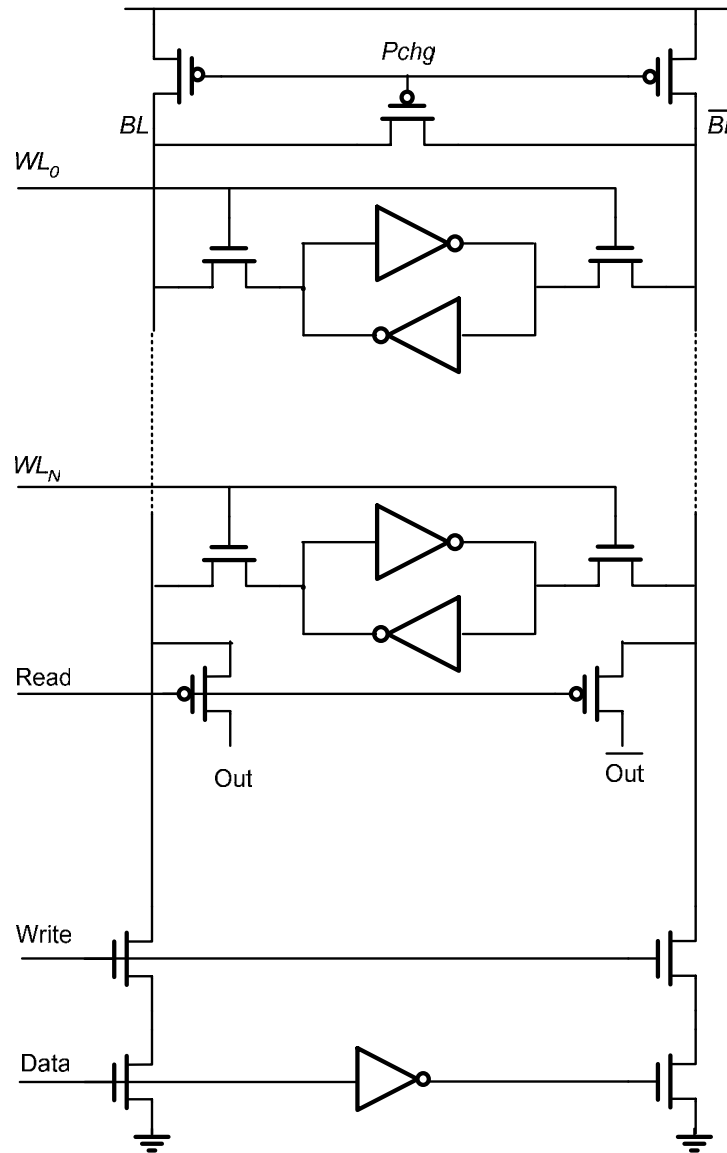


Figure 1: SRAM column.

You don't have to include the sense amplifier in this phase. Size the precharge, read and write access transistors to ensure read and write functionality of the column. Verify the DRC and LVS correctness of the design and simulate the write and read operation of the memory.

2. Decoder Design

Design (on paper, no simulation) a 6-to-64 memory decoder for use with your memory array. The input loading of each of the true and complementary address lines is constrained to be less than $3fF$. The output loading of the decoder is determined from the wordline loading of the memory cells (extracted from phase I) and the wireload (estimated by hand). The length of the wordline can be determined from the horizontal dimension of the cell, see Figure 2.

The decoding is performed in two phases: predecoding of 3 input bits and the final row decoding of 2 bits. The predecoder drives the final decoders together with the wire that whose length equals the height of the memory array.

The goal is to minimize the delay of the decoder. Keep in mind that in the next phase, the decoder layout has to match the SRAM word pitch.

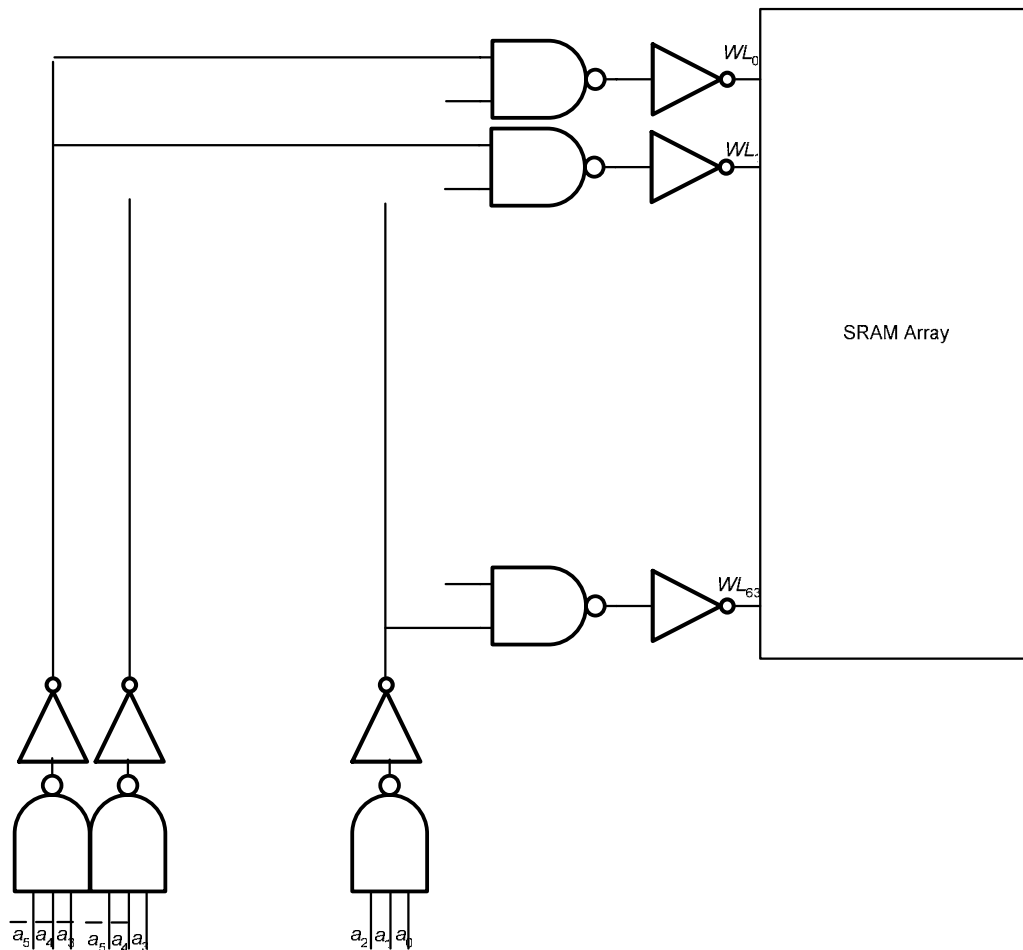


Figure 2: SRAM decoder.

4. Report

The total report should not contain more than three pages. You are not allowed to add any other sheets. The organization of the report should be based on the following outline:

Cover page: Names, project title, summary of the parameters that include the estimated decoder delay.

Page 1: Annotated schematic and the layout of the SRAM bitline. Simulation of the read and write operation.

Page 2: Schematic of the decoder. Capacitance estimates. Description of the sizing procedure.

Grading:

30%	Approach and correctness
30%	Results
30%	Report
10%	Creativity