UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
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Borivoje Nikolić ***FALL 2004 TERM PROJECT PHASE I*** *EECS 141*

1. Designing a 64x32-bit memory array – Background

Memory arrays are an essential building block of all digital systems. In this semester's project, we will design a memory array that consists of 64 32-bit words.

1.1. High level structure

A block diagram of a memory array is shown in Figure 1.

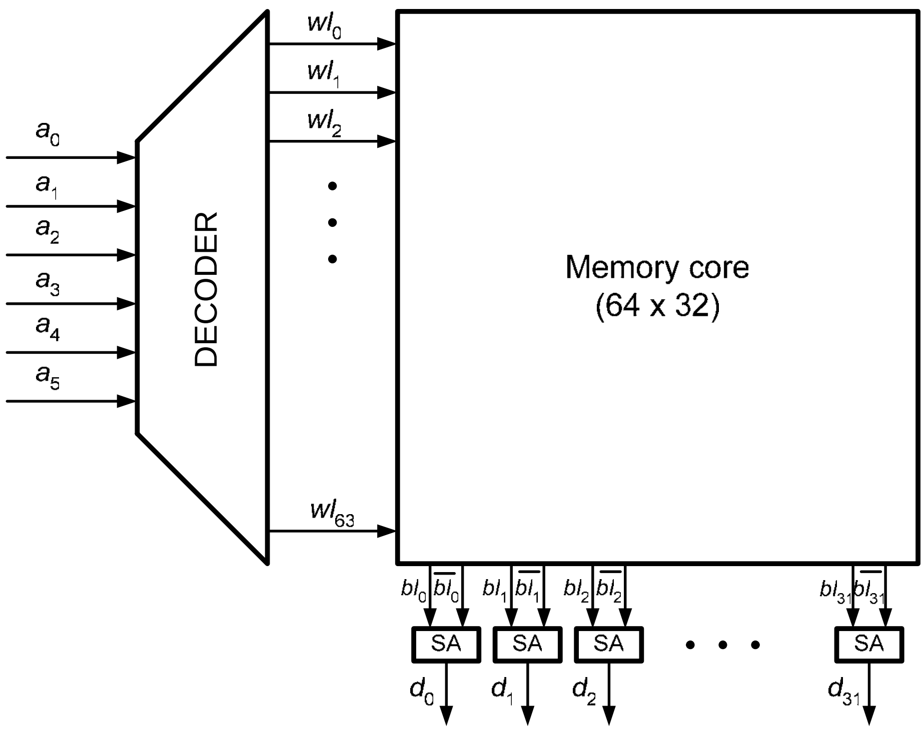

Figure 1. SRAM array block diagram.

There are three major parts:

- Address decoder: The address decoder takes in 6 address lines, provided as true and complement values a_5-a_0 and a_5-a_0 and produces 64 select signals wl_{63}-wl_0.
- SRAM array: Consists of an array of 64 x 32 6-transistor SRAM cells.
- Sense amplifiers: There is one sense amplifiers per column that amplifies the SRAM cell outputs. There are no column decoders – 32-bit words are addressed.

In addition to these blocks the array also has a circuitry that allows writing the data and precharging the bitlines to V_{DD} before the read operation, which is not shown in figure.

2. Implementation and Constraints

The goal of this project is to design a functional, compact and fast memory for use in high-performance or mobile microprocessor with a particular set of optimization criteria. The project will be completed in FOUR phases.

PHASE 1, due Tuesday, November 2, at 5pm.

In the first phase of the project, you will design a 6-transistor static memory cell. The goal is to design a stable memory cell with minimum size. To guarantee functionality, the cell should be sized to prevent the voltage rise higher than 0.4V at the storage node during the read operation (the bitlines are precharged to V_{DD} before the read operation).. The cell writeability must be guaranteed by sizing of devices that drives the storage node below 0.4V during the write process.

PHASE 2, due Tuesday, November 9, at 5pm.

Design (pencil and paper) of the 6-64 memory decoder. The input loading of each of the true and complementary address lines is constrained to be less than 3fF. The output loading of the decoder is determined from the wordline loading of the memory cells and the wireload. The length of the wordline can be determined from the horizontal dimension of the cell.
The decoding is performed in two phases: predecoding of 3 input bits and the final row decoding of 2 bits. The predecoder drives the final decoders together with the wire that whose length equals the height of the memory array.

PHASE 3, due Tuesday, November 23, at 5pm.

The complete decoder in schematic and layout. Note that decoder pitch in layout has to match the SRAM pitch.

PHASE 4, due Tuesday, December 6, at 5pm.

Design of the sense-amplifier. Assembly of the complete SRAM array and post-layout simulation.

PROJECT POSTERS, Tuesday, December 6, 9:30-11am.

In each phase of the design you will turn in a short report. A longer report, together with a poster presentation is due on December 6.

Physical and electrical specifications:

2.1. TECHNOLOGY: The design is to be implemented in a 0.25 μm CMOS process with 5 metal layers. You should use only up to 4 metal layers for the SRAM design. The SPICE technology is in the g25.mod file.

2.2. POWER SUPPLY: You are free to choose any supply voltage and logic swing up to 2.5 V. Make sure that you use the appropriate model when you perform any hand analysis.

2.3. PERFORMANCE METRIC: The propagation delay for static CMOS design is defined as the time interval between the 50% transition point of the inputs and the 50% point of the worst-case output signal. Make sure you pick the worst-case condition and state EXPLICITLY in your report what that condition is.! Note that the delay definitions might be different for the sense-amplifiers.

2.4. AREA: The area is defined as the smallest rectangular box that can be drawn around the design. Since the SRAM must interface with the rest of the chip, all inputs and outputs must be accessible from the boundary of the block.

2.5. NAMING CONVENTIONS: The input operands of the memory are named *a*<5:0>. The output data is *d*<31:0>. Wordline and bitline signals are labeled as *wl*<63:0> and *bl*<31:0>.

2.6. REGISTERS: You don't need to use any registers in this design.

2.7. CLOCKS: You will need only one clock for the sense amplifiers. Remember that the load capacitance of the clock should be included in the energy analysis.

2.8. V_{OH}, V_{OL}, NOISE MARGINS: You are free to choose your logic swing in the decoder. The noise margins should be at least 10% of the voltage swing. Test this by computing the VTC between one of the inputs and the output signals (with the other outputs set to the appropriate values) for a static design. For a dynamic circuit, apply an input signal with a 10% noise value added to the input and observe the outputs.

2.9. RISE AND FALL TIMES: All input signals have rise and fall times of 50 ps. The rise and fall times of the output signals (10% to 90%) should not exceed 200ps.

2.10. LOAD CAPACITANCE: Your output is driving a 20fF load at each output.

2.11. INPUT CAPACITANCE: Each address input should not load the previous stage with more than 3fF (less is OK).

The goal is to minimize the **area** of a **functional** array. **Delay** and **power** should also be minimized.

3. Simulation

Analyze the circuit by hand. Also use HSPICE to simulate the design and prove that it functions correctly. You will need to determine the input pattern that causes the worst-case propagation delay or energy consumption by analyzing your circuit schematic.

4. Report

The quality of your report is as important as the quality of your design. Be sure to provide all relevant information and eliminate unnecessary material. **Organization, conciseness, and completeness are of paramount importance.** Do not repeat information we already know. Use the templates provided on the web page (Word and PDF formats). Make sure to fill in the cover-page and use the correct units. Turn in the reports for each phase in the homework drop box.
In addition, mail an electronic version of your final report and the poster as a Word or PDF file to ee141-project@bwrc.eecs.berkeley.edu. You will be also asked to provide your final netlist.

4.1 Report for phase 1

Your report should discuss your overall design philosophy and the important design decisions made at the circuit and layout level. Discuss why your approach guarantees stability and minimizes the area while increasing the operating speed or reduces the energy. Provide estimates of your results and describe how you arrived at them. Describe the sizing methodology used in your design.

The total report should not contain more than two pages. You are not allowed to add any other sheets. The organization of the report should be based on the following outline:

Cover page: Names, project title, summary of parameters that include the cell area and static noise margin.

Page 1: Annotated schematic and the layout of the SRAM cell. Simulation of the static noise margin and the voltages at the storage nodes during read and write operations. Brief description of design decisions should accompany the graphs.

Remember, a good report is like a good layout: it should perform its function (convey information) in the smallest possible area with the least delay and energy (to the reader) possible.

The quality of the report is an important (major) part of the grade!

The total project grade is divided into five parts, four phases of the project and the final report/poster, each carrying 20% of the total grade.
For each of the four phases, the grade will be divided as follows:

- 30% Approach and correctness
- 30% Results
- 30% Report
- 10% Creativity