

EE 141 Spring 2008 Homework #4

Problem 1: Inverter Delay

Simulate a 5-stage ring oscillator shown below with different loads on each node. Set the supply voltage to 1V and measure the oscillation frequency, f_{OSC} , and the average current, I_{AVE} , drawn by the inverters in the chain from the supply.

Each inverter is minimum sized: $W_n = 120 \text{ nm}$, $W_p = 240 \text{ nm}$, $L_n = L_p = 100 \text{ nm}$.

Note that the current drawn by the inverters used as loads should not be included in I_{AVE} . Note that $N = (\text{Fan Out} - 1)$ and the capacitor values are 2fF.

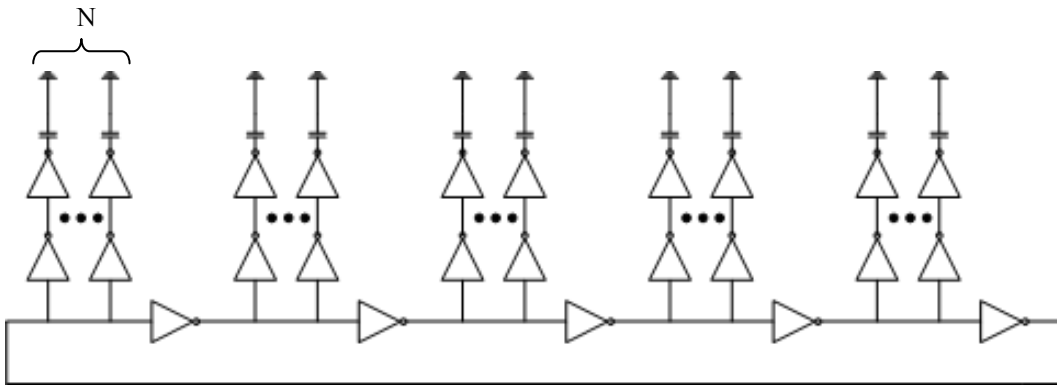
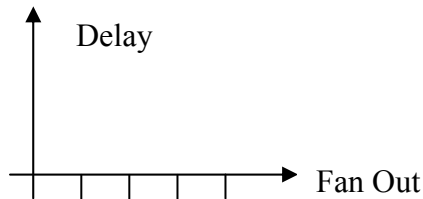


Figure 1. The 5-stage CMOS Ring Oscillator. Note that $N = (\text{Fan Out} - 1)$ and the capacitor values are 2fF.

- a. Determine the propagation delay of each inverter for under the following conditions and plot the propagation delay versus the number of inverter loads.

Inverter Load (Fan Out)	Propagation Delay
1	$t_{p1} = ?$
2	$t_{p2} = ?$
3	$t_{p3} = ?$
4	$t_{p4} = ?$



- b. From the data in part a, determine t_{p0} .
- c. Determine the parameter γ , where $\gamma = C_{INT}/C_G$.
- d. Determine C_{INT} and C_G .
- e. Determine R_{EQ_ave} .

Simulation hint: To ensure that your ring oscillator starts to oscillate and not stay in a meta-stable state, use the initial condition option command in the Analog Environment window. Select *Simulation* \rightarrow *Convergence Aids* \rightarrow *Initial Condition...* and select the node you will be observing to have an initial value of 0V.

Problem 2: Buffer Sizing

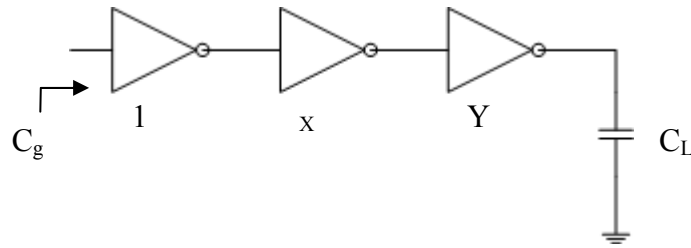


Figure 2. A 3-stage inverter chain driving a load C_L .

The supply voltage is 1V and $\gamma = 0.7$ for the 3-stage inverter chain given above.

- What is the minimum value of C_L that this inverter chain can drive optimally?
- What is the delay, X and Y at this minimum C_L ?
- What is the maximum value of C_L that this inverter chain can drive optimally?
- What is the delay, X and Y at this maximum C_L ?
- If $C_L = 100 C_g$, what is the X and Y needed for minimum delay?
- How many stages are needed to drive a $C_L = 100 C_g$ for minimum delay?
- What is this minimum delay for $C_L = 100 C_g$?

Problem 3: Scaling

A 90-nm CMOS microprocessor runs has a clock frequency of 3.2 GHz at a 1.2 volt supply voltage and consumes 103 watts of power. It has a die area of 122 square millimeters and has 125 million transistors. Assume short-channel devices and ignore second order effects like mobility degradation, series resistance, etc.

- What is the power density of this microprocessor?
- Using general scaling and maintaining a clock frequency of 3.2 GHz, what will the power, power density and area of the processor if it is scaled to a 65-nm CMOS process using a 1-volt supply voltage?
- How fast can the new 65-nm microprocessor be clocked using a 1 volt supply, without exceeding the power consumption of the original 1.2 V, 90-nm implementation? Assume that power is the limiting factor and not performance.