EE 141 Spring 2008 HW4 Solutions

Problem 1:

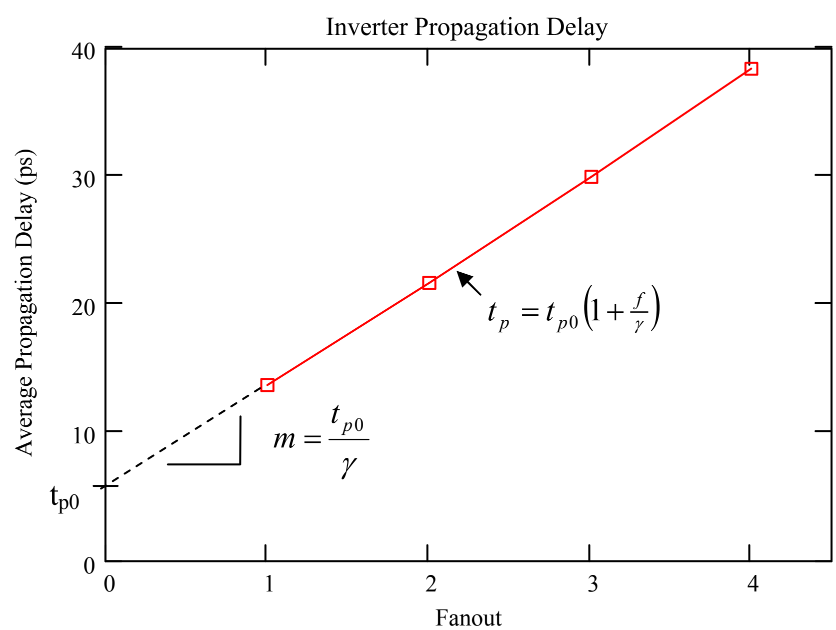
Simulation Results:

Fan Out, (FO)	Oscillation Frequency, (f_{OSC})	Average Current, (I_{AVE})
1	$f_1 = 7.27$ GHz	$I_1 = 48.11\ \mu A$
2	$f_2 = 4.63$ GHz	$I_2 = 49.12\ \mu A$
3	$f_3 = 3.34$ GHz	$I_3 = 48.88\ \mu A$
4	$f_4 = 2.60$ GHz	$I_4 = 48.69\ \mu A$

The average propagation delay of each inverter can be computed using $f_n = \frac{1}{2N \cdot t_{pn}}$, where $N = 5$. The average power can also be computed as $P_{AVE} = V_{DD} I_{AVE}$ with $V_{DD} = 1V$.

Fan Out, (FO)	Propagation Delay, (t_p)	Average Power, (P_{AVE})
1	$t_{p1} = 13.74$ ps	$P_1 = 48.11\ \mu W$
2	$t_{p2} = 21.57$ ps	$P_2 = 49.12\ \mu W$
3	$t_{p3} = 29.88$ ps	$P_3 = 48.88\ \mu W$
4	$t_{p4} = 38.43$ ps	$P_4 = 48.69\ \mu W$

Plotting t_p versus FO:



Taking the y-intercept of the best-fit line gives a t_{p0} of 5.31 ps. The slope of this line, *m*, gives a γ value of 0.645.

Using the average power values obtained from the simulation, the total switched capacitance can be obtained from $P_{AVE} = C_{Total} V_{DD}^2 f$.

Note that $C_{Total,n} = 5(C_{INT} + nC_G) = 5(\gamma C_G + nC_G) = 5C_G(\gamma + n)$ and $\gamma = 0.645$. Tabulating the results give:

Fan Out, (FO)	Total Switched Capacitance	Gate Capacitance
1	6.61 fF	0.8 fF
2	10.59 fF	0.8 fF
3	14.60 fF	0.8 fF
4	18.71 fF	0.8 fF

Thus, C_G = 0.8 fF and consequently, since $C_{INT} = \lambda C_G$, C_{INT} = 0.52 fF.

Using $t_{p0} = \ln(2) R_{eq,ave} C_{INT}$, we can estimate $R_{eq,ave}$ = 14.78 kΩ.

Problem 2:

The minimum load capacitance that can be driven by the 3-stage inverter chain such that it is still faster than a 2-stage inverter chain can be found by equating their delays:

$$2\left(1+\frac{\sqrt{F_{\min}}}{\gamma}\right)=3\left(1+\frac{\sqrt[3]{F_{\min}}}{\gamma}\right)$$

Note that $F=\frac{C_L}{C_G}$ and $\gamma = 0.7$. This results in $F_{min} = 18.86$.

The normalized delay is then $D_1=3\left(1+\frac{\sqrt[3]{F_{\min}}}{\gamma}\right)=14.41\cdot t_{p0}$.

The optimal values of X and Y can be expressed as $X=f_1=2.66$ and $Y=f_1^2=7.08$. Note that $f_1=\sqrt[3]{F_{\min}}$.

The maximum load can be found when the delay for a 3-stage inverter chain becomes the same as for a 4-stage inverter chain:

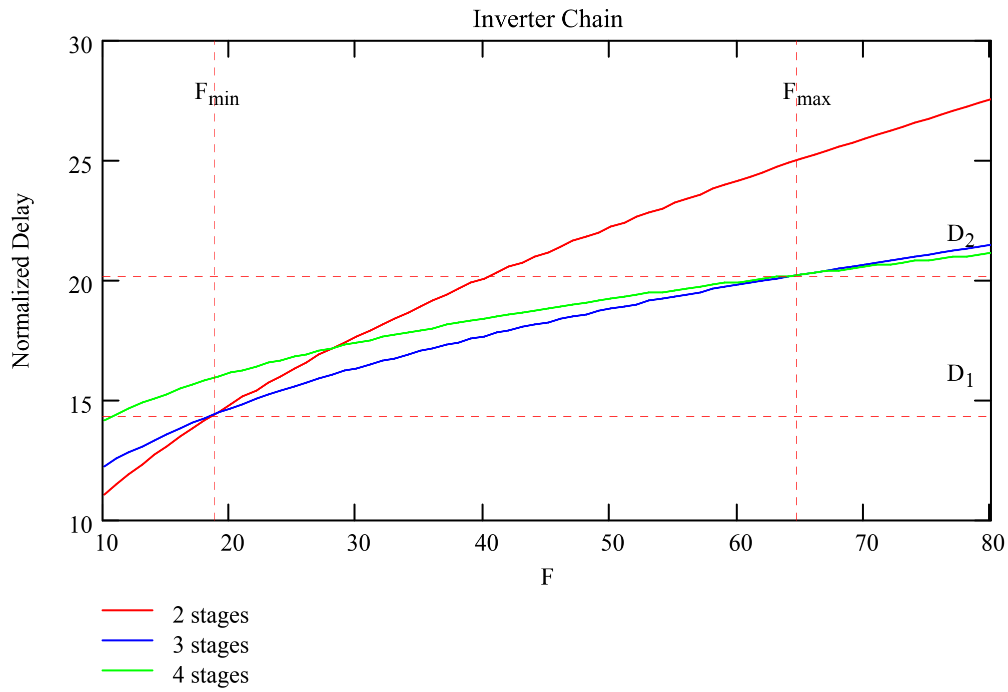
$$3\left(1+\frac{\sqrt[3]{F_{\max}}}{\gamma}\right)=4\left(1+\frac{\sqrt[4]{F_{\max}}}{\gamma}\right)$$

This results in $F_{max} = 64.75$.

The normalized delay is then $D_2=3\left(1+\frac{\sqrt[3]{F_{\max}}}{\gamma}\right)=20.21\cdot t_{p0}$.

The optimal values of X and Y can be expressed as $X=f_2=4.01$ and $Y=f_2^2=16.12$. Note that $f_2=\sqrt[3]{F_{\max}}$.

A plot of the delays for 2-, 3- and 4-stage inverter chains are shown below, showing the region where a 3-stage inverter chain has the best performance.



For C_L = 100 C_G, F = 100, and the minimum delay is when $f = \sqrt[3]{100} = 4.64 = X$ and $Y = f^2 = \left(\sqrt[3]{100}\right)^2 = 21.54$.

The minimum delay when driving 100 C_G is then $D = 3\left(1 + \frac{f}{\gamma}\right) = 22.89 \cdot t_{p0}$.

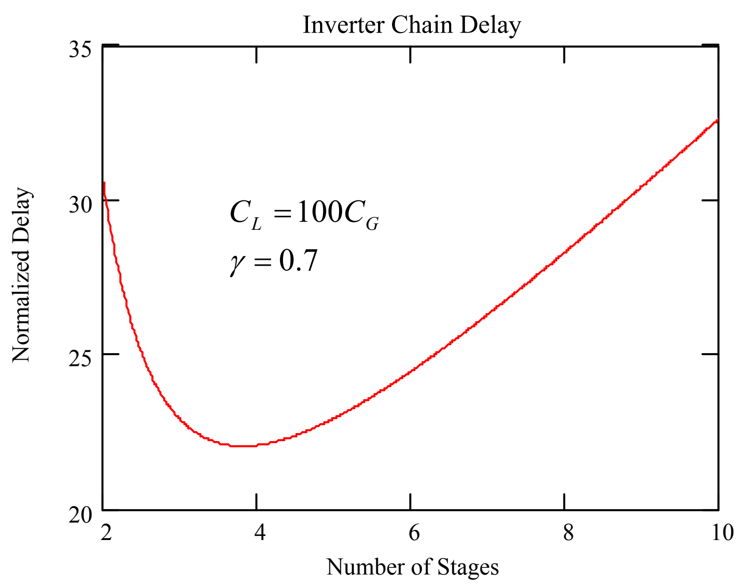
The minimum delay for N stages can be expressed as:

$$D(N) = N\left(1 + \frac{\sqrt[N]{100}}{\gamma}\right)$$

Taking the derivative of this expression (using numerical methods might be easier) and equating it to zero gives the optimum number of stages to get minimum delay. Thus, $\frac{\partial D(N)}{\partial N} = 0$ gives N = 3.8. Which we then round it off to N = 4.

Using 4 stages, we obtain $D(4) = 22.07 \cdot t_{p0}$.

The plot below shows the relationship between the delay and the number of stages for $C_L = 100C_G$.



Problem 3:

The power density is just the total power over the area of the chip.

This results in $PD_{90nm} = \frac{P_{90nm}}{A_{90nm}} = \frac{103\,W}{122\,mm^2} = 844\frac{mW}{mm^2}$.

For the general scaling case, $S = \frac{90\,nm}{65\,nm} = 1.385$ and $U = \frac{1.2\,V}{1\,V} = 1.2$.

Thus, $A_{65nm} = \frac{A_{90nm}}{S^2} = 63.63\,mm^2$ and $P_{65nm} = \frac{P_{90nm}}{S \cdot U^2} = 44.77\,W$. The power density is then $PD_{65nm} = \frac{P_{65nm}}{A_{65nm}} = \frac{44.77\,W}{63.63\,mm^2} = 0.7\frac{W}{mm^2}$.

For equal power consumption in the 90-nm and 65-nm case,

$$P_{90nm} = P_{65nm}$$
$$C_{90nm}V_{90nm}^2 f_{90nm} = C_{65nm}V_{65nm}^2 f_{65nm}$$

Therefore, the frequency of the scaled $f_{65nm} = S \cdot U^2 \cdot f_{90nm} = 6.38\,GHz$.