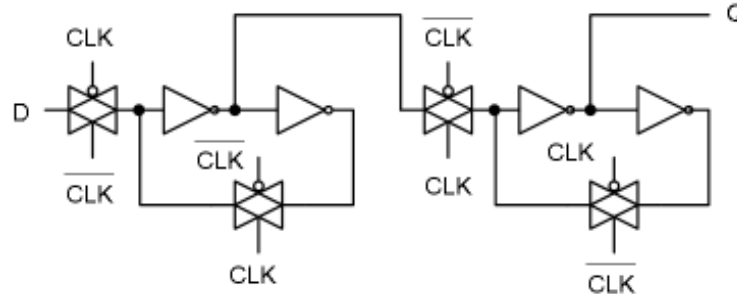
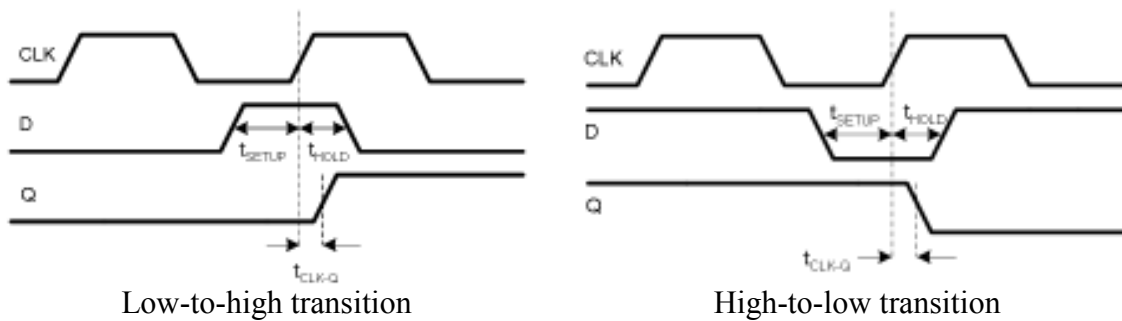


**EE 141 Spring 2008 Homework #7 Due Monday, April 21, 2008**  
 Flip-flop Characterization

Part 1. Given the master-slave flip flop below:

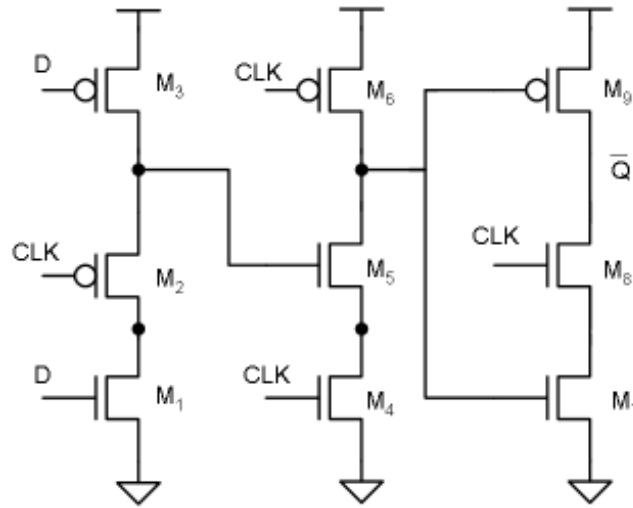


The inverters (minimum sized) are sized with  $W_n = 120\text{nm}$ ,  $W_p = 240\text{nm}$ . The transmission gates are sized as:  $W_{n,TG} = 120\text{nm}$  and  $W_{p,TG} = 240\text{nm}$ . All lengths are  $100\text{nm}$  and  $V_{DD} = 1\text{V}$ . The timing definitions are shown in the figure below:



- Analytically determine the rising and falling **characteristic CLK-to-Q delay**, assuming that the D and CLK inputs are driven by a minimum sized inverter and the Q output is driving four minimum sized inverters.
- Simulate the FF and verify the CLK-to-Q delays. Use at least 200 ps of setup and hold times to eliminate their effects on the CLK-to-Q delays. These are known as the **characteristic CLK-to-Q delays**. ( $t_{\text{CLK-Q,HL}}$  and  $t_{\text{CLK-Q,LH}}$ )
- Determining the setup time: Using simulation, reduce the setup time until the CLK-to-Q delay increases by 10% or when the flip-flop fails to latch the data, whichever is larger. Note that the hold time should be kept constant and greater than 200 ps. This is the **setup time**,  $t_{\text{SETUP}}$  (the larger of the two cases: low-to-high or high-to-low). Record and report this quantity. What happens as the setup time is reduced further?
- Determining the hold time: Using simulation, reduce the hold time until the CLK-to-Q delay increases by 10% or when the flip-flop fails to latch the data, whichever is larger. Note that the setup time should be kept constant and greater than 200 ps. This is the **hold time**,  $t_{\text{HOLD}}$  (the larger of the two cases: low-to-high or high-to-low). Record and report this quantity. What happens if the hold time is reduced further?

Part 2. Repeat this characterization for the TSPC flip flop given below.

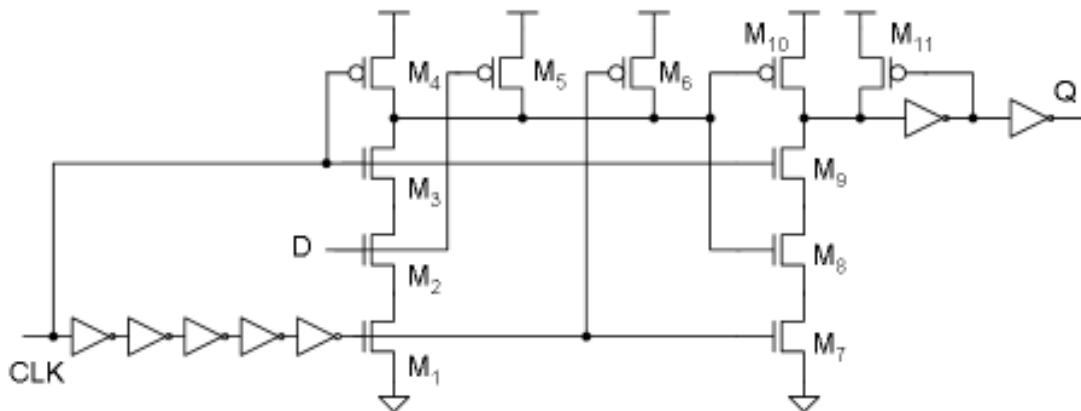


A positive edge triggered TSPC flip-flop.

Transistor widths:  $M_1 = 120\text{nm}$ ,  $M_2 = M_3 = 480\text{nm}$ ,  $M_4 = M_5 = M_7 = M_8 = 240\text{nm}$ ,  $M_6 = M_9 = 240\text{nm}$ . All lengths are  $100\text{nm}$  and  $V_{DD} = 1\text{V}$ .

Part 3.

a. Repeat this characterization for the pulse-based flip flop given below.



A pulse-based dynamic flip-flop.

Transistor widths:  $M_1 = M_2 = M_3 = M_7 = M_8 = M_9 = 360\text{nm}$ ,

$M_4 = M_5 = M_6 = M_{10} = 240\text{nm}$ ,  $M_{11} = 120\text{nm}$ .

The inverters are sized  $240\text{nm}/120\text{nm}$  and all lengths are  $100\text{nm}$  and  $V_{DD} = 1\text{V}$ .

- What is the purpose of the 5 inverters in series?
- What is the purpose of  $M_{11}$ ?