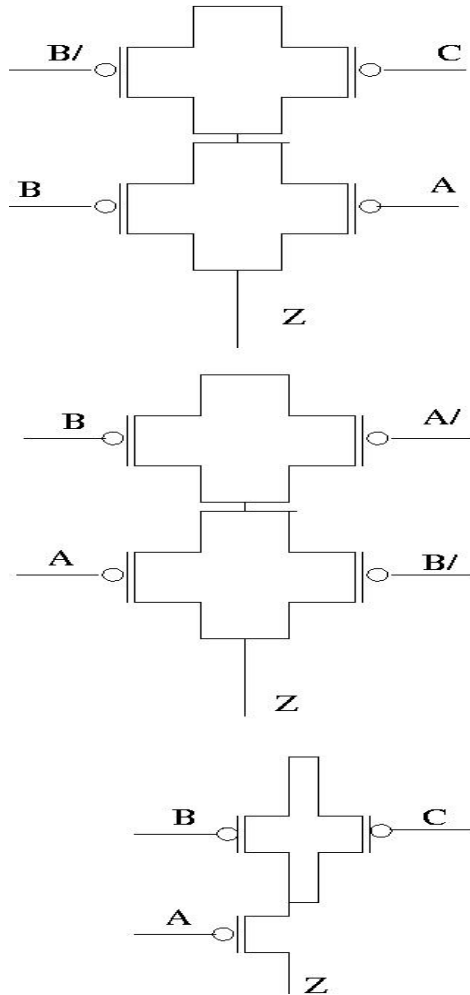


EE141 HW5 Solution-Spring 2008

P1) The functionalities are for (a)  $Z = AB + C(\overline{B})$ , for (b)  $Z = A(\overline{B}) + (\overline{A})B$ , for (c)  $Z = A + BC$ . The pull up networks are shown below.



P2) The expression can be simplified noting that  $C(\overline{D}) + CD = C(D + \overline{D}) = C \cdot 1 = C$  so that the expression becomes either

$$Z = \overline{(\overline{A} / B / C)}$$

or the equivalent

$$Z = A + B + C$$

Expression 1 is NAND-based and therefore will have lower delay. Let us perform logical effort analysis: the chain has no branching, so  $B = 1$ . Similarly,  $F = 64$  and  $G = 5/3$  (This is the

logical effort for a three input NAND). The total effort is  $64 * 5/3 = 106$  and therefore the per-stage effort should be  $106^{0.5} = 10.32$ . As a result, the inverter driving strength should be  $10.32X$  and the input inverters should be sized for unit strength.

P3)

For a) since the XORs are symmetric gates, they have  $p_0 = p_1 = 0.5$  at their outputs., so  $p_{0 \rightarrow 1} = 1/4$ . For the NAND gate, the probability of the output being at one is the probability that both inputs will be at 1 at the same time and so for this case (symmetric inputs)  $p_1 = 1/4$  and  $p_{0 \rightarrow 1} = 3/16$ .

So  $P_d = 1/4 f_s V_{dd}^2 (C_1 + C_2 + 3/4 C_3)$

For b) similarly, we have  $p_1 = 1/8, p_0 = 7/8$  so that  $p_{0 \rightarrow 1} = 7/64$  and  $P_d = 7/64 C f_s V_{dd}^2$

For c) the activity at the output of the NAND gate is calculated as before as  $3/16$ , while that at the output of the OR gate requires more care. In particular, since the input to the gate are both equally likely to be 0 or 1, we need to use the fact that the output of an OR gate is 0 if and only if both inputs are 0. Therefore

$p_0 = p_{0a} * p_{0b} = 3/4 * 1/2 = 3/8$  and  $p_{0 \rightarrow 1} = 15/64$ . The total power is  $P_d = f_s V_{dd}^2 (15/64 C_1 + 3/16 C_2) = f_s V_{dd}^2 (C_1 + C_2) 7/64 (15/7 * C_1 / (C_1 + C_2) + 12/7 * C_2 / (C_1 + C_2)) > f_s V_{dd}^2 (C_1 + C_2) 3/16 > f_s V_{dd}^2 (C_1 + C_2) 7/64$ . Therefore the implementation with a single NAND gate is more power efficient for this capacitance distribution.

Intuitively, the switching activity of the 3-NAND is the lowest of all gates, which is why the power is lowest.