

Homework #2  
Spring 2008

**Problem 1: VTC**

An idealized digital gate has a voltage transfer characteristic shown in figure

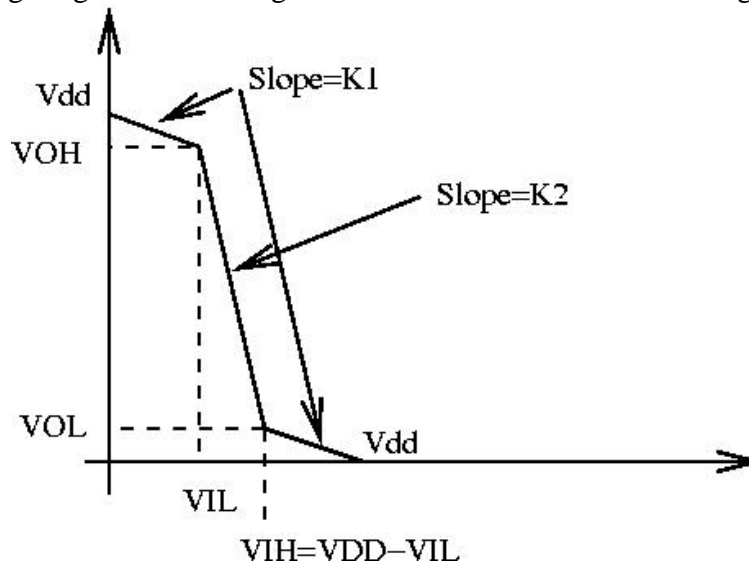


Figure 1: Inverter Piecewise Linear VTC

- Dictate conditions on  $K1$  and  $K2$  such that the gate is a useful digital gate
- Choose now  $K1=.5, K2=10$ . Calculate  $V_{IH}$  and the noise margins.
- Draw the VTC for a cascade of two such gates and calculate the noise margin.
- What would happen if the gate did not have the regenerative property as you try to cascade several of them?

**Problem 2: Multistage delay**

A simple model of a CMOS inverter is given by a two switches with finite on-resistance and a capacitor as shown in Figure 2.

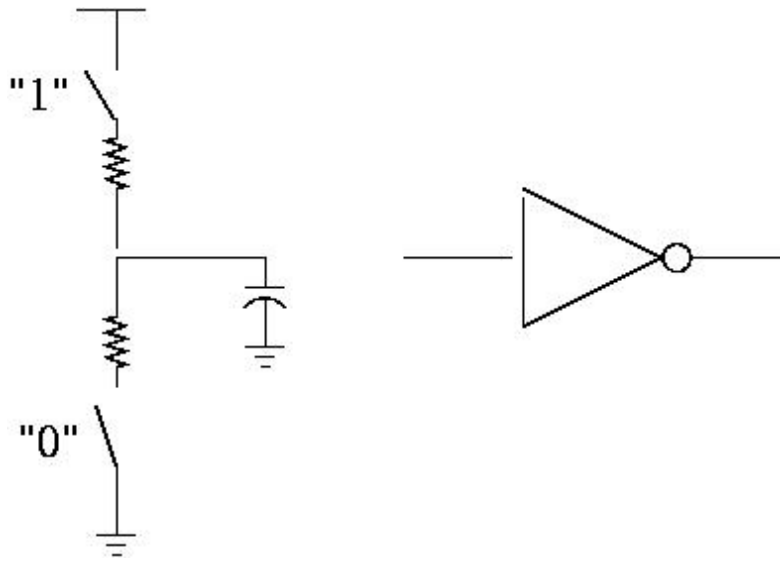


Figure 2: Switch Model for CMOS inverter

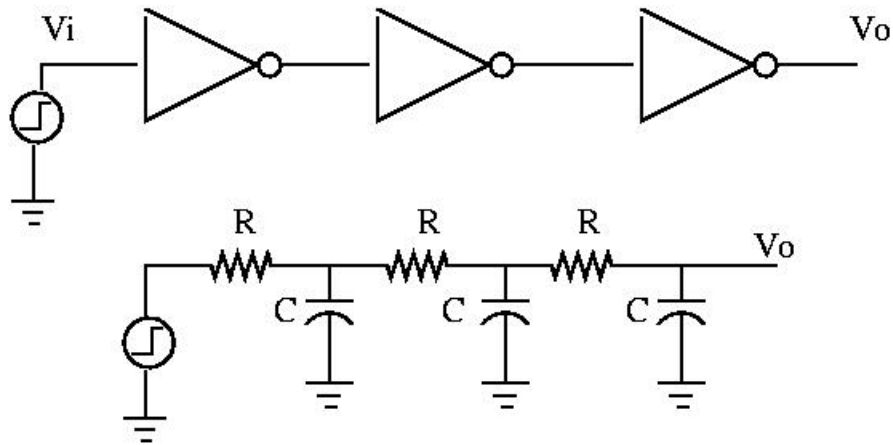


Figure 3: Three stage logic delay model

- Calculate the delay 50% in- 50% out delay of this network assuming the input is an ideal step and the resistor and capacitor value are known.
- Repeat the calculation for a third-order network, obtained cascading three first order sections. You can use approximations (i.e. open circuit time constants) to solve for the dominant time constant of the circuit.
- Does this model provide an accurate result for the circuit of figure 2? Why or why not?

## Problem 3: $I_d$ - $V_{gs}$ MOS Model

Setup a simple simulation test-bench to measure the  $I_d$ - $V_{gs}$  curves of an NMOS and a PMOS device. Use .4um/90nm devices for both NMOS and PMOS.

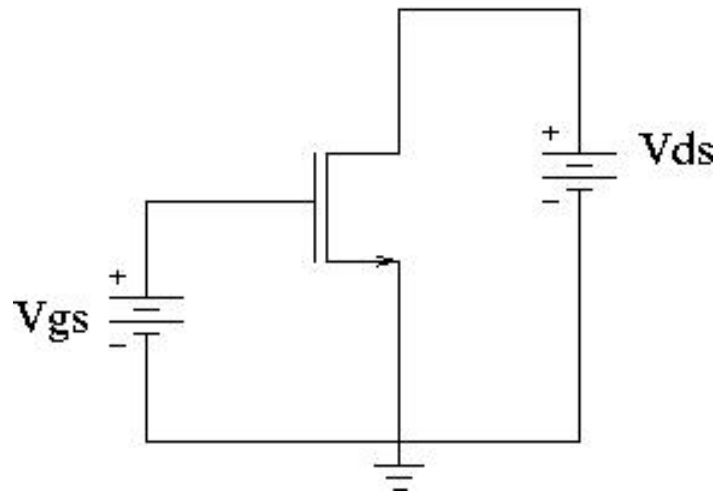


Figure 4: MOS simulation setup for Problem 3

- Plot  $I_d$ - $V_{gs}$  curves using a y-semilog plot for different values of  $V_{ds}$ . Calculate the subthreshold slope  $n$  for NMOS and PMOS.
- From a linear scale  $I_d$ - $V_{gs}$  graph, extract threshold variations as a function of  $V_{ds}$ . The threshold voltage is usually defined as the intercept of the extrapolated  $I_d$ - $V_{gs}$  curve in strong inversion with the zero axis (see plot for a more information).

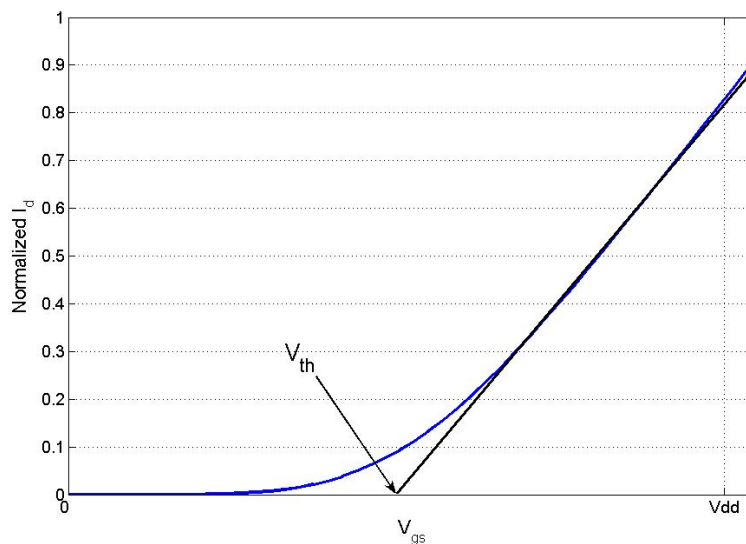


Figure 5:  $V_{th}$  Extraction example

Create a linear model of  $V_{th}$  as a function of  $V_{ds}$  and plot the resulting data. You can do this characterization work for NMOS only, but extract the threshold for at least one  $V_{ds}$  point also for PMOS.

Deliverables:

1. Plots of  $I_d$ - $V_{ds}$  and  $\log(I_d)$ - $V_{gs}$  obtained from simulations.
2. Plot of  $V_{ds}$ - $V_{th}$

Please, make clear the steps you follow in your simulation. Imagine you are part of a design team and I am your colleague in Italy and we want to agree on a common model to use for our design and a stable parameter extraction methodology. Try to enable me to take your report, run the simulations and obtain the same results you obtained.