

University of California at Berkeley
College of Engineering
Department of EECS

Jan M. Rabaey

Spring 2008

EE141

Homework #3

Due: Friday, Feb. 15th, 5 pm 240 Cory

Problem 1: Unified MOS Transistor Model

Similar to the work you did for Problem 3 of Homework 2 you are now trying to determine the parameters for the unified MOS transistor model.

- 1) Setup a simulation to create a set of I_D - V_{DS} curves for an NMOS transistor of the technology we are using with the following parameters:
W/L: 0.12um / 0.1 um
 V_{GS} : 0.2, 0.3, 0.6, 0.9 and 1.2 V
 V_{DS} : from 0 to 1.2 V
 V_{BS} : 0 (basically connect the bulk node of the transistor to its source)
Extract V_{T0} , λ , k' and V_{VSAT} (sometimes also referred to as V_{DSAT}).
- 2) Next you should compare how well the unified MOS model with the parameters you extracted matches simulations. To do that, use the Calculator (choose Tools \rightarrow Calculator in the waveform window) to export the simulation result into a .csv file so that you can import it into Excel or Matlab. You can do so by enabling the family button in the calculator window (highlighted in blue in Fig 1) and clicking on a curve in the waveform window. After that your calculator should look like shown in Fig. 1. Then click on the table icon right next to "Append" and on top of "Eval" (highlighted in red in Fig 1). Another window pops up that allows you to chose the parameters for the table you are about to create. Choose something similar to what is shown in Fig. 2) and confirm by clicking ok. A table containing numerical results of your simulation pops up and you can "Save as" that table as a .csv file, which can be conveniently be opened by e.g. Excel. Import the data in Excel or any other tool of your choice and compare it to the results you obtain by using the unified model with the parameters you derived in part 2 (in excel e.g. you can make use of the function "min"). If you do everything correctly you will end up with something similar to Fig 3. You may actually tune the parameters you obtained in part 2 a bit to get a better match. Which part of the curves do you want to match best if you are mainly concerned with estimating the delay of inverters?

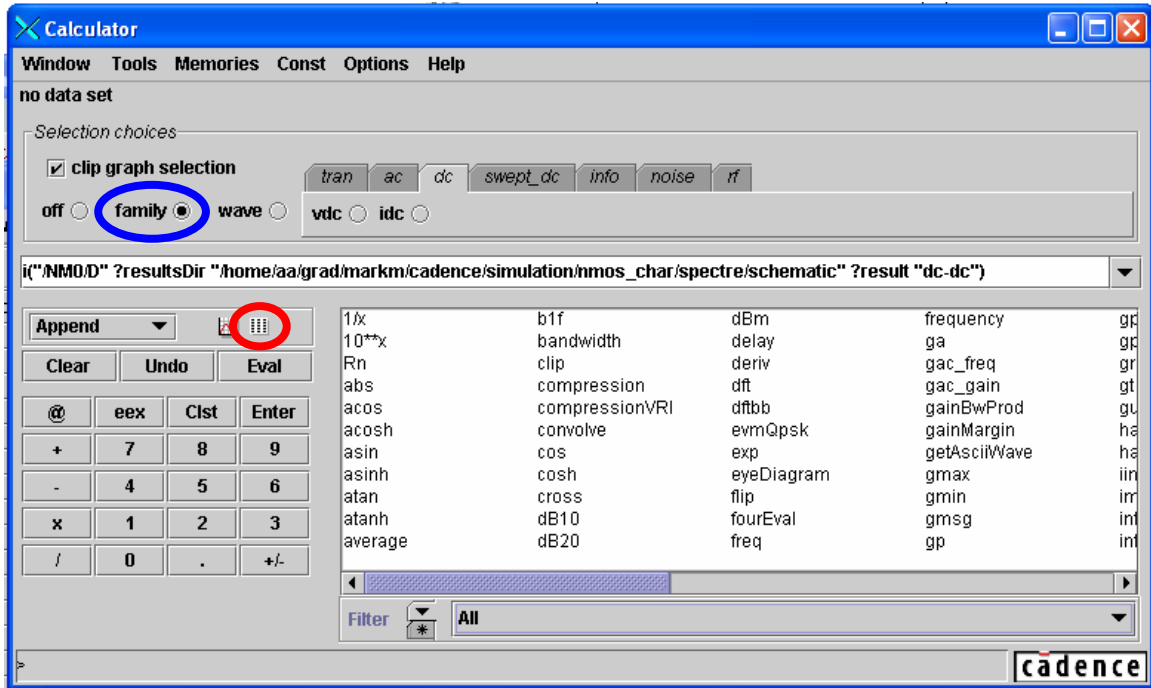


Figure 1: Using the Calculator to export simulation results

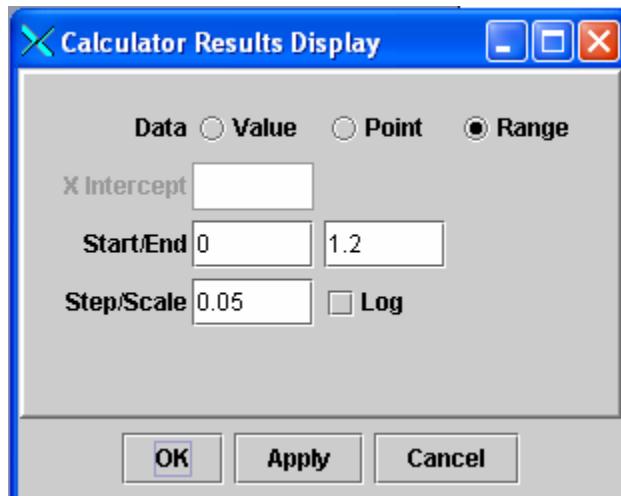


Figure 2: Choosing settings for table

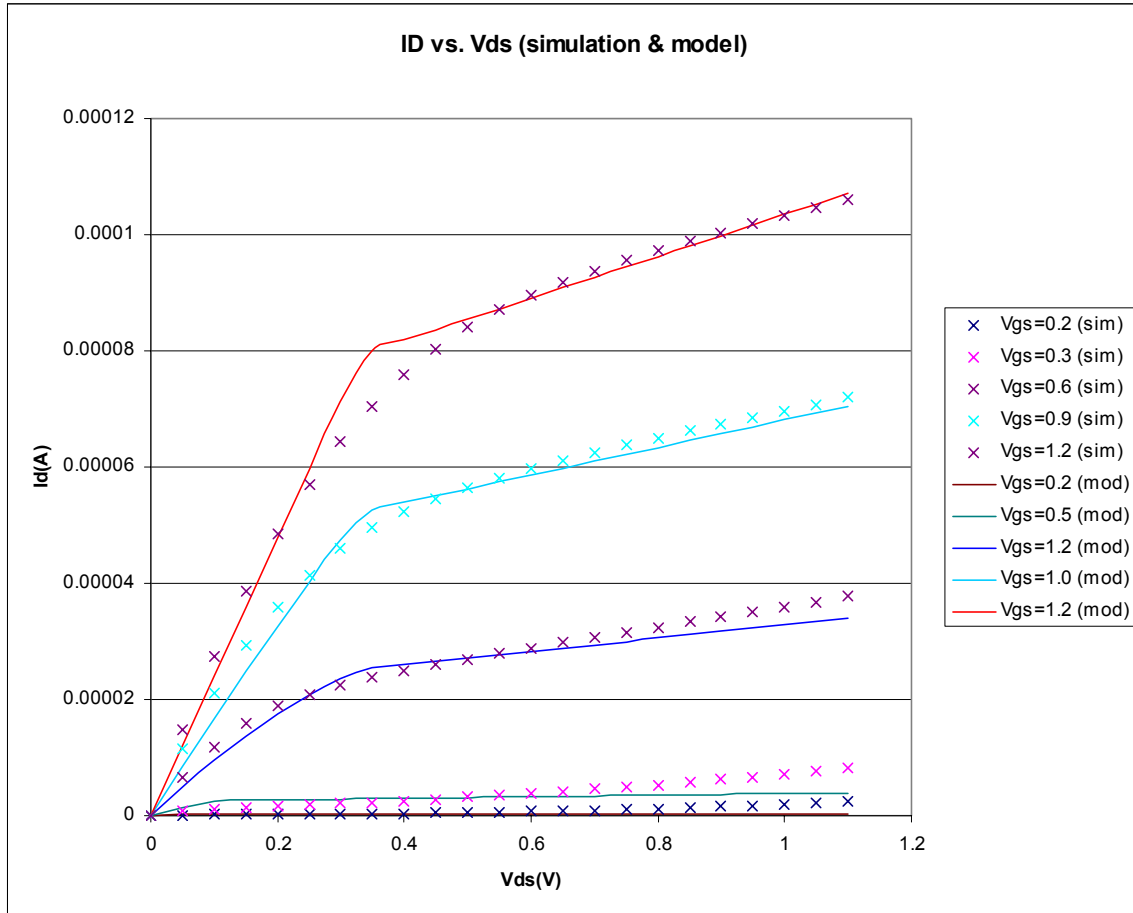


Figure 3: Example for comparison of simulation and unified model

- 3) Repeat steps 1 and 2 for a PMOS with the same transistor size and V_{GS} values of 0.3, 0.4, 0.6, 0.9 and 1.2 V. You don't have to do part 3 again but of course you are welcome to do so.

Deliverables: Provide plots of the simulations (NMOS and PMOS), a summary of your extracted values based on the simulations (NMOS and PMOS) as well as the comparison of the simulation and your modeling effort (only NMOS required, but feel free to submit the PMOS plots as well in case you did them). Provide also the set of parameters you used to create the comparison, in case you tweaked your parameters to achieve a better fit.

Problem 2: VTC

As mentioned in class, inverters do not always have to be made out of a PMOS on top of an NMOS. One example of an inverter using a resistor instead of a PMOS is shown in Figure 4.

- 1) Explain briefly why the given circuit is an inverter. Name one major drawback of this inverter.
- 2) Calculate V_{OH} , V_{OL} and V_M of the circuit in Figure 4. (Assume $R = 10\text{k}\Omega$ and $W/L = 5 \cdot 0.120\ \mu\text{m} / 0.1\ \mu\text{m}$)

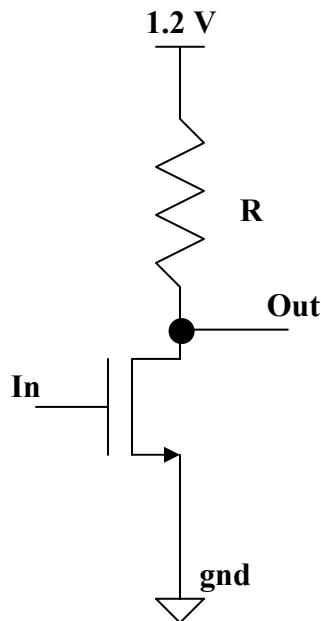


Figure 4: Inverter based on NMOS and resistor

Imagine now your company is considering cutting down the costs of their logic process by using an NMOS only process. Your boss asks you to design an inverter consisting only of NMOS transistors and to evaluate its performance. To make matters even worse he asks you to use only two device sizes: A minimum device ($120\text{nm}/100\text{n}$) and a device which is 5 times wider ($5 \cdot 120\text{n}/100\text{n}$). The only nice thing about the process they are planning on implementing is that it allows you to tie the bulk of the transistors to wherever you want.

- 3) First you start out by drawing the schematic of a NMOS-only inverter. (You are basically trying to replace the resistor of the inverter of Figure 4 by another NMOS transistor)
- 4) Then you perform some first order hand calculations to estimate the VTC of your circuit. To do so you calculate V_{OH} , V_{OL} , V_M , the inverter gain at V_M as well V_{IL} , V_{IH} . When carrying out the hand calculations you use the unified transistor model and the parameters you obtained for the 90 nm technology you obtained in Problem 1.

- 5) Next, you simulate your circuit and compare the results to your hand calculations. Does the result of your first order calculation matches simulations reasonably well? If not, what could be the reason for that?
- 6) Finally you provide some feedback to your boss in terms of at least 3 good points why using such a technology is not such a good idea after all. (Hint: You might want to compare the NMOS-inverter to the one you simulated in Homework 1)

In your homework provide the schematic of your NMOS-only inverter, your hand calculations, a plot comparing simulated and calculated VTC and the feedback to your boss

Problem 3: Inverter Delay Estimation

In this problem you are asked to estimate the FO-4 delay of the inverter you simulated in Homework 1 (NMOS: 0.12/0.1 and PMOS 0.24/0.1) for a supply voltage of 1.2V. You can assume that the inverter switches at $V_{DD}/2$.

- 1) First you calculate the equivalent CL at the output of the inverter. Use the following technology parameters to calculate the various capacitances:

$$\begin{aligned}
 C_{ox} &= 14.8 \text{ fF}/\mu\text{m}^2 \\
 C_{gdn} &= C_{gson} = 0.378 \text{ fF}/\mu\text{m} \\
 C_{jon} &= 0.798 \text{ fF}/\mu\text{m}^2 \\
 m_j &= 0.222 \\
 C_{jswon} &= 0.0479 \text{ fF}/\mu\text{m} \\
 m_{jsw} &= 0.01 \\
 \Phi_0 &= 0.9 \\
 C_{gdop} &= C_{gsop} = 0.355 \text{ fF}/\mu\text{m} \\
 C_{jop} &= 0.791 \text{ fF}/\mu\text{m}^2 \\
 m_j &= 0.331 \\
 C_{jswon} &= 0.0479 \text{ fF}/\mu\text{m} \\
 m_{jsw} &= 0.01
 \end{aligned}$$

- 2) Next calculate the equivalent resistances for the N- and the PMOS (again use the unified transistor model with the parameters you obtained from problem 1)
- 3) Based on these results, what is the FO-4 delay of your inverter?
- 4) Compare your result with simulation. How well do they match? What are some possible reasons for mismatch (in case there is any)