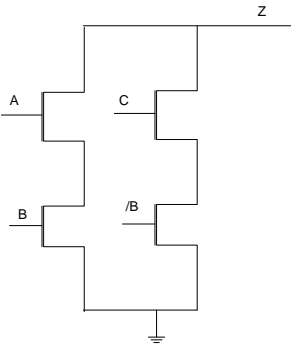
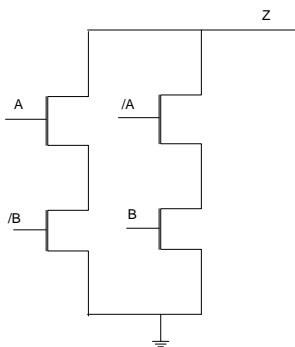


1) For each of these gates (all implemented in static CMOS), complete the schematic and write the corresponding logic function.

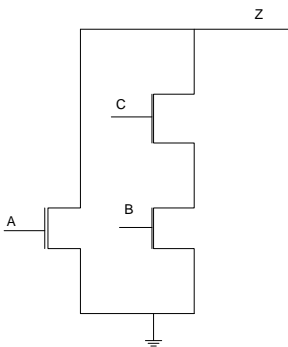
I.



II.



III.



2

a) Synthesize using static CMOS the following logic function using 2 stages of logic (+1 inversion if needed).

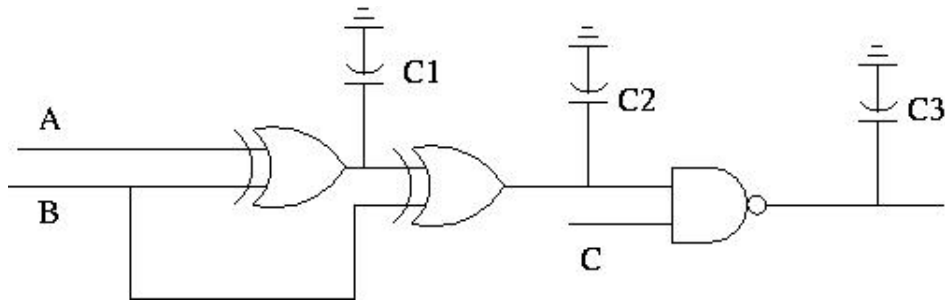
$$Z = \overline{\overline{(A+B)} \cdot (\overline{C} \cdot \overline{D} + CD)}$$

b) Size the stages for optimal delay using logical effort analysis for a 64 Unit Inverter fanout.

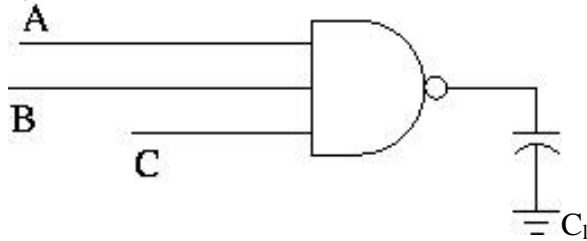
3)

For each of the following gates, assume all the inputs are random variables on  $\{0,1\}$  with  $p_0=p_1=1/2$ . Assume there is no spatial correlation (i.e. all the inputs are independent) and no temporal correlation (i.e. inputs at time  $k$  are independent of inputs at time  $j$  different than  $k$ ). Calculate the power dissipation as a function of the capacitor values (ignore the gates intrinsic capacitors) and the clock frequency  $f_S$ .

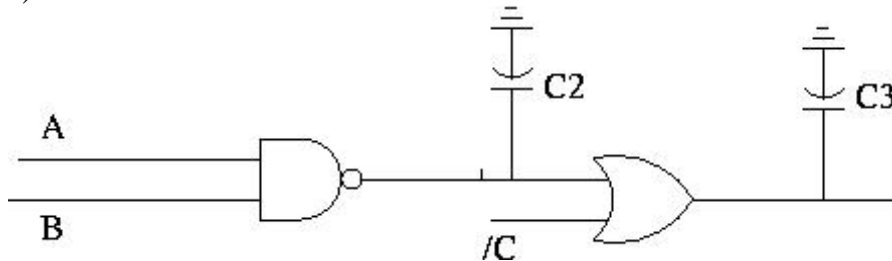
a)



b)



c)



Notice that b) and c) both implement a three input NAND. Assuming  $C_2+C_3=C_1$  What is the lower power implementation?