

University of California at Berkeley  
College of Engineering - Department of EECS

Jan M. Rabaey

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EE141

Homework #6

Due: Friday, April 4th, 5 pm 240 Cory

**Problem 1: Complex Logic**

Figure 1 shows the block diagram of a digital circuit with two standard inverters and two complex logic gates. The details of the two complex logic gates are shown in Figure 2.

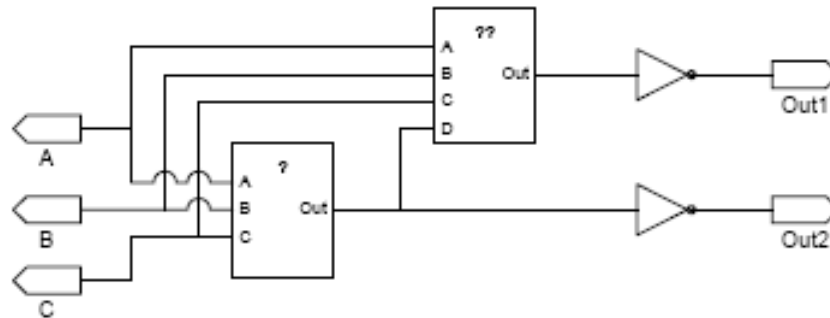


Figure 1: Block diagram of unknown logic circuit

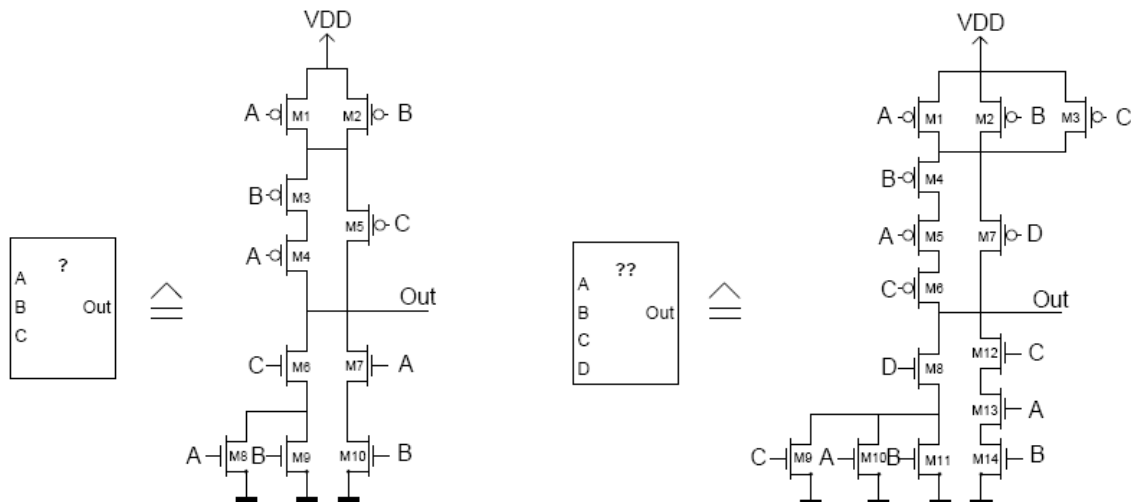


Figure 2: Transistor level schematic of logic gates in circuit of Figure 1.

- 1) Express Out1 and Out2 in terms of the input signals A, B and C.  
What functionality does the circuit implement?

- 2) Size all the transistors in Figure 2, such that the gates “?” and “??” have a worst case pull-up and pull-down performance approximately equal to a unit sized inverter. When doing so try to minimize the maximum input capacitance seen at any input. Assume long channel devices, use integer ratios when scaling the devices and neglect body effect.
- 3) Calculate the logical effort of all the inputs of gates “?” and “??”
- 4) Which input propagates fastest to the output Out2? Considering your answer to 1), could there be any reason for giving that particular input priority?

## Problem 2: Static CMOS vs. Pass-Transistor Logic

In this problem you are asked to compare static CMOS vs. Pass-Transistor Logic (PTL) based on a XNOR gate. A XNOR (Figure 3 shows the symbol) provides a high output signal whenever the two input signals are logically equal.



Figure 3: Symbol of XNOR

- 1) Design a 2-input XNOR in static CMOS. To simplify matters you can assume that you have both input polarities available ( $A$  &  $A'$ ,  $B$  and  $B'$ ). How many transistors do you need to build the XNOR?
- 2) Now design the same circuit in NMOS only PTL (no CMOS inverter at the output). Again, assume that both input polarities are available. How many transistors do you need now?
- 3) Next you use the gates you just designed to build the circuit shown in Figure 4. You implement the same circuit one time using the CMOS XNOR gate and the second time using your PTL XNOR gate. You can assume that somehow magically you have the inverted output values of your single gates available as well (i.e. if Output = low =  $V_{OL}$  then Output' = high =  $V_{OH}$  and vice versa). Further assume  $V_{DD} = 1.2$  V,  $V_{Th} = V_{Tp} = 0.3$  V and neglect body effect.
  - a. Complete the timing diagram in Figure 5
  - b. By purely looking at the voltage levels, which implementation would you prefer and why?
  - c. Compare the two implementations with respect to their performance (elaborate).
  - d. Propose a solution utilizing NMOS and PMOS that helps to overcome some of the problems of the less favorable logic style. What are the pros and cons of your solution?

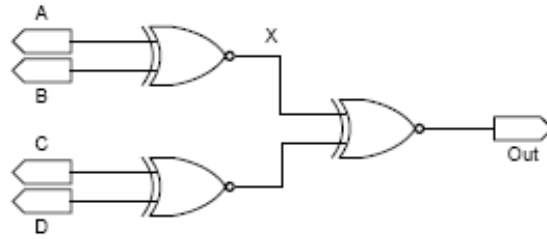


Figure 4: Cascade of XNORs

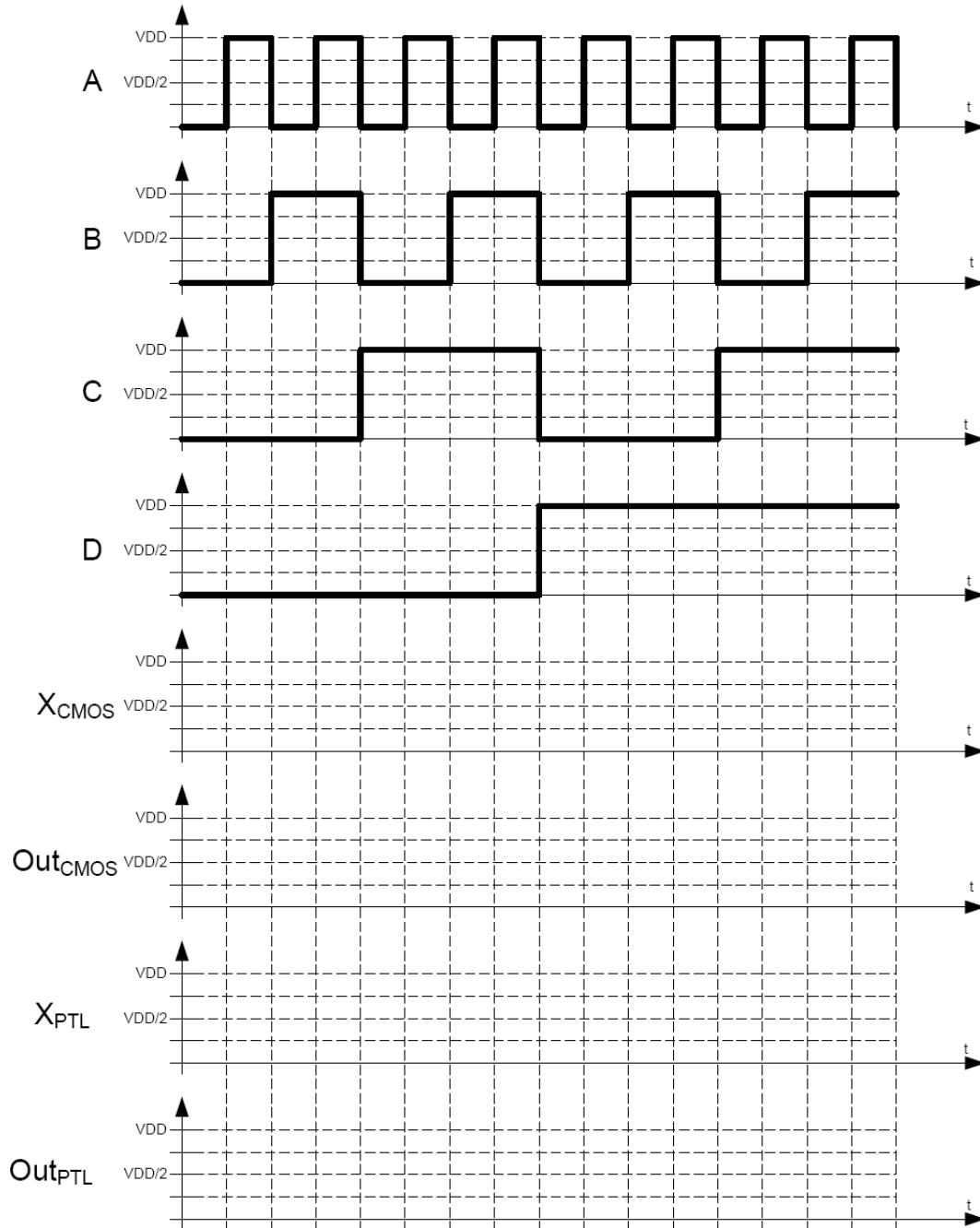


Figure 5. Timing diagram for circuit in Figure 4.

### Problem 3: Dynamic Logic

- a) Implement the logic function given below with a single dynamic logic gate and optimize it with the fact that the input A is part of the critical path in mind.

$$\text{Out} = \overline{A(B+C)}$$

- b) Draw the VTC (i.e.  $V_{\text{out}}$  vs.  $V_A$ ) for the case when B and C are high all the time and A transitions from low to high during the evaluation cycle. Assume  $V_{\text{DD}} = 1.2 \text{ V}$  and  $V_{\text{Tn}} = 0.3 \text{ V}$
- c) Size the input transistors (the ones that are not connected to the clk-signal; the “clk-transistors” can be considered to be ideal shorts during the evaluation cycle for this problem) such that the gate has the same pull down strength as a minimum inverter. Calculate the logical effort for your gate for a high-to-low transition at the output. Does your result make sense?
- d) Assume an equivalent  $C_L = 30 \text{ fF}$  and  $C_S = C_D = 2 \text{ fF}$  (for the used transistor size, i.e. you don't need to multiply it by your scaling factor from c). Calculate the output voltage at the end of the evaluation cycle assuming B and C are low all the time and A transitions from low to high during the evaluation cycle. Assume that  $f_{\text{clk}}$  is slow enough such that all the transients settle within the evaluation period.
- e) In order to combat the effect of charge sharing you can add a circuit shown in Figure 6 (often referred to as inverter + level restoring transistor or keeper) to the output of your dynamic gate.
- Why do you think the size of the inverter is 4/1 instead of the usual 2/1? Does that make sense or is it a mistake?
  - What is the maximum  $W_K/L_K$  of the keeper transistor that still guarantees full functionality of your gate?  
 $(V_{\text{DD}} = 1.2 \text{ V}, V_{\text{Tn}} = V_{\text{Tp}} = 0.3 \text{ V}, k_n' = 180 \text{ uA/V}^2, k_p' = 90 \text{ uA/V}^2, \lambda_n = \lambda_p = 0.5, V_{\text{satn}} = 0.3 \text{ V}, V_{\text{satp}} = 0.6 \text{ V}, \text{min. W/L} = 0.12/0.1 \text{ um})$

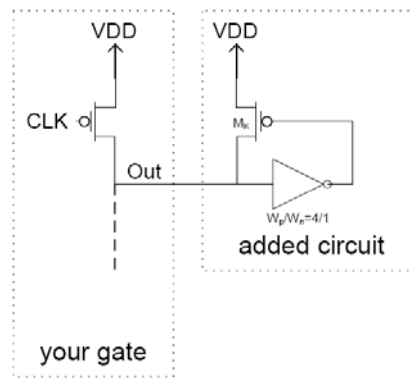


Figure 6: Circuit add-on to mitigate effect of charge sharing