

University of California at Berkeley
College of Engineering - Department of EECS

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EE141

Homework #8

Due: Monday, May 5th, 5 pm 240 Cory

Problem 1: Timing and Race Conditions

The following circuit consists of a source portion, which adds the outputs of two registers R1 & R2 and a destination portion, which stores the sum in R3. The connections between the source and the destination are made by an automatic router, which creates wires with an average length of 1mm and containing an average of 10 contact holes in series. This leads to a resistance of about 100 Ω and capacitance of about 50 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3. Each register presents a load of 300 fF to the clock driver.

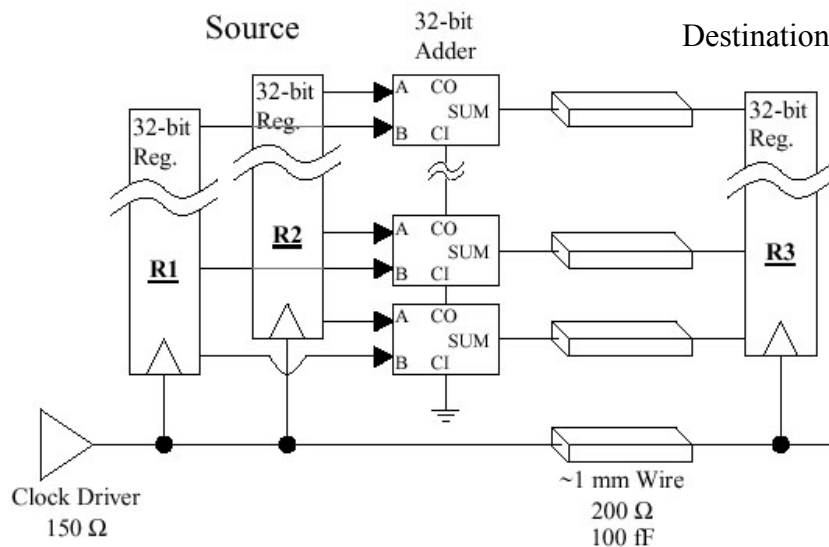


Figure 1: High level diagram of problem 1

Assume the following timing values for the logic: $t_{\text{carry}} = 30$ ps, $t_{\text{sum}} = 50$ ps (including the wire load), $t_{\text{setup}} = 50$ ps, $t_{\text{hold}} = 25$ ps, $t_{\text{clk-Q}} = 40$ ps.

- a) Does this circuit have a race problem? What is the minimum clock period?
- b) What if the driver were placed at the destination? Would there be a race problem? What would the new minimum clock period be?

Problem 2: Wires & Elmore Delay

Figure 2 shows a clock distribution network on a digital chip. Each wire (indicated as box) is about 0.1 mm long and has the same characteristics as the wires in problem 1. The ends of the clock distribution network are connected to 32-bit registers which again represent a load of 300 fF. Further, you can assume that the input clock signal is a perfect square wave. Calculate the maximum clock skew between any of the register blocks.

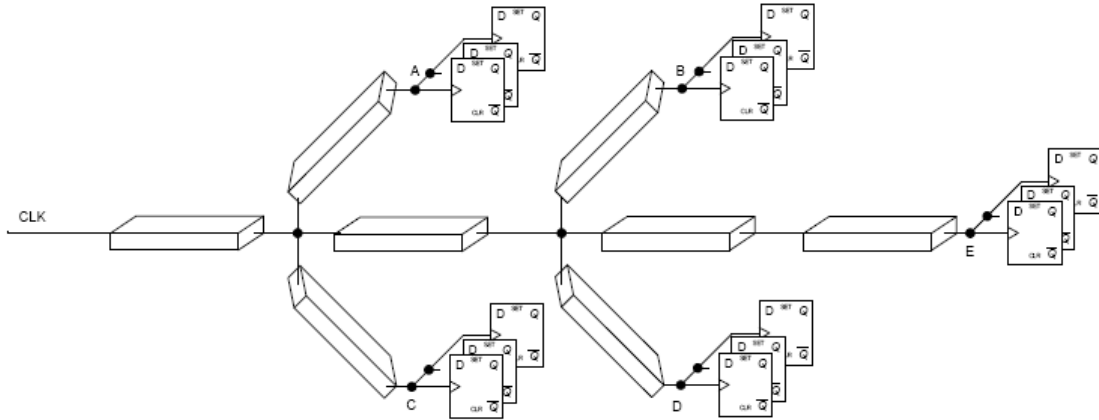


Figure 2: High level diagram of problem 2

Problem 3: Transmission Line

A inverter sized up by 50 compared to a minimum sized inverter in our 90 nm technology (remember: R_{req} is approx. 10kOhm for a minimum sized inverter) is used to drive a capacitor via a 5 mm long and 1 μm wide Aluminum wire. The wire has a sheet resistance of 50 mOhm/ μm , a capacitance of 50 aF/ μm^2 and a fringing cap of 40 aF/ μm . The wire can be approximated as a lossless transmission line and the capacitor at the output can be considered as an open-ended termination for all practical purposes. VDD is equal to 1.2 V for this problem and you can neglect all parasitic capacitances associated with the driving inverter.

- Determine the propagation delay of the circuit (for the high to low transition at the input). You may assume that the transmission line effect is dominant. Draw the lattice diagram and the V_{out} waveform during the transition (V_{out} from VDD to VDD/2)
- Size up the inverter such that the delay is minimized

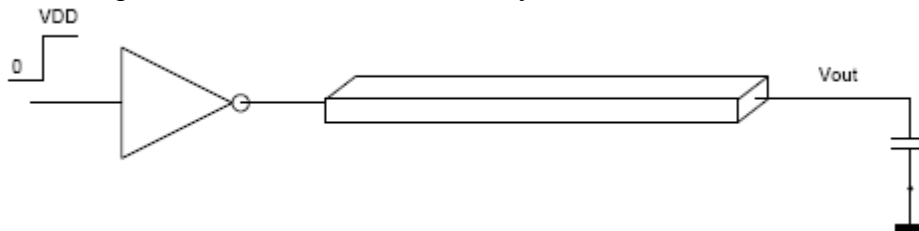


Figure 3: High level diagram of problem 3