University of California at Berkeley
College of Engineering - Department of EECS

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Solutions Homework #8

Due: Monday, May 5th, 5 pm 240 Cory

Problem 1: Timing and Race Conditions

The following circuit consists of a source portion, which adds the outputs of two registers R1 & R2 and a destination portion, which stores the sum in R3. The connections between the source and the destination are made by an automatic router, which creates wires with an average length of 1mm and containing an average of 10 contact holes in series. This leads to a resistance of about 100 Ω and capacitance of about 50 fF for each wire.

A clock driver buffers the clock signal at the source and is routed by the same tool to the destination, where it connects to R3. Each register presents a load of 300 fF to the clock driver.

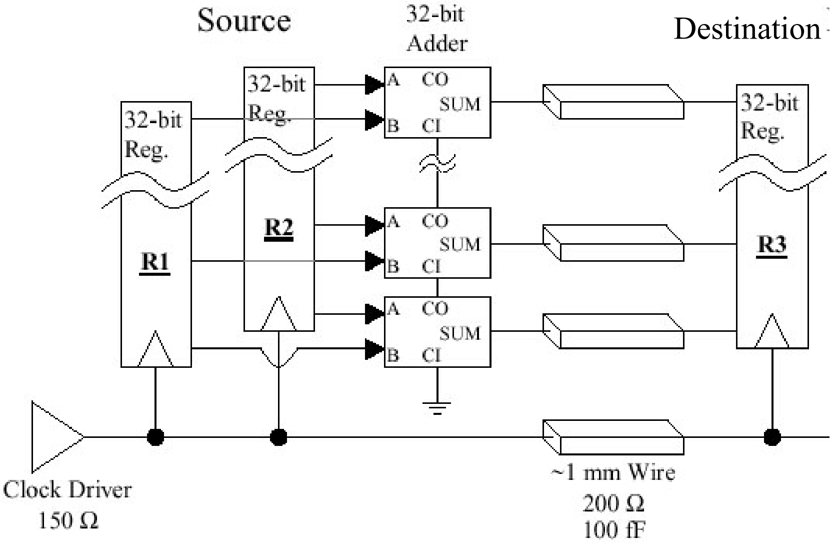
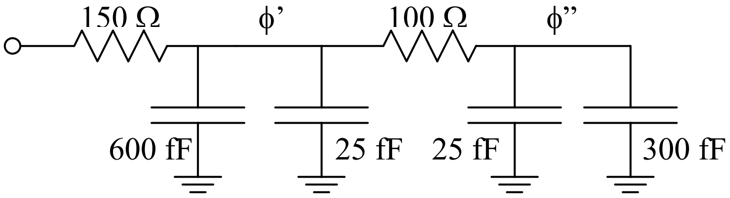


Figure 1: High level diagram of problem 1

Assume the following timing values for the logic: $t_{carry} = 30$ ps, $t_{sum} = 50$ ps (including the wire load), $t_{setup} = 50$ ps, $t_{hold} = 25$ ps, $t_{clk\text{-}Q} = 40$ ps.

a) Does this circuit have a race problem? What is the minimum clock period?

First, we need to find the skew between the source register clock (ϕ') and the destination register's clock (ϕ"). We can do this with a π2 model of the wire and the Elmore delay model.



$t_{\phi'} = 0.69\ [150 \text{ x } (625\text{ f} + 325\text{ f})] = 98.33\text{ ps}$

$t_{\phi''} = 0.69\ [\ (150 \text{ x } 625\text{ f} + (150{+}100) \text{ x } 325\text{ f}\ ] = 120.75\text{ ps}$

$\delta = t_{\phi''} - t_{\phi'} = 22.42\text{ ps}$

Next, we check the race condition to see if the circuit will work properly. Note that the minimum logic delay is a single sum.

$t_{hold} + \delta \leq t_{clk\text{-}Q} + t_{sum}$ (eq. 10.4 from textbook)

$25 + 56.1 \leq 40 + 50$

$22.42\text{ ps} \leq 90\text{ ps}$ TRUE ... Thus, this circuit has no race problem

Lastly, we find the minimum clock period. Note that the maximum logic delay is a single sum plus the delay of the carry chain.

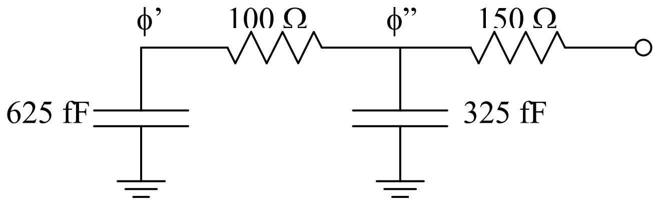
$T \geq t_{clk\text{-}Q} + (31\ t_{carry} + t_{sum}) + t_{setup} - \delta$ (eq 10.3 from textbook)

$T \geq 40 + 31 \text{ x } 30 + 50 + 50 - 22.42$

$T \geq 10.48\text{ ns}$

b) What if the driver were placed at the destination? Would there be a race problem? What would the new minimum clock period be?

Identical to (a), except that the clock in driven in the other direction.



$t_{\phi''} = 0.69 \text{ x } 150 \text{ x } (325\text{ f} + 625\text{ f}) = 98.33\text{ ps}$
$t_{\phi'} = 0.69\ [\ 150 \text{ x } 325\text{ f } + (150+100) \text{ x } 625\text{ f}] = 141.5\text{ ps}$
$\delta = t_{\phi''} - t_{\phi'} = -43.17\text{ ps}$

$t_{hold} + \delta \leq t_{clk\text{-}Q} + t_{sum}$
$25 - 43.17 \leq 40 + 50$
$-18.17 \leq 90$ TRUE ... Thus, no race problem
Note that this circuit has a higher margin

$T \geq t_{clk\text{-}Q} + 31\ t_{carry} + t_{sum} - \delta + t_{setup}$
$T \geq 40 + 31 \text{ x } 30 + 50 + 18.17 + 50$
$T \geq 10.88\text{ ns}$
Note that the minimum cycle time is now longer then in the previous case

Note: it is acceptable to use a T model instead of the π model. For parts a the π model delays the first register's clock with extra capacitance at its clock input, giving a more optimistic skew, while the T model is more pessimistic. The T model would give a skew that is 0.69*100*25f = 1.725 ps worse, but shorten the minimum clock period by as much. Part b) would see the opposite effect.

Also, the wording was ambiguous as to whether t_{sum} is the delay to the far end of the line to the register, or just to the output of the adder. The above solution assumed the former, but it's acceptable to interpret t_{sum} as the latter, in which case an interconnect delay of 0.69*100*25f=1.725 ps should be added to t_{sum}. This helps the race condition check, but increases the minimum clock period.

Problem 2: Wires & Elmore Delay

Figure 2 shows a clock distribution network on a digital chip. Each wire (indicated as box) is about 0.1 mm long and has the same characteristics as the wires in problem 1. The ends of the clock distribution network are connected to 32-bit registers which again represent a load of 300 fF. Further, you can assume that the input clock signal is a perfect square wave. Calculate the maximum clock skew between any of the register blocks.

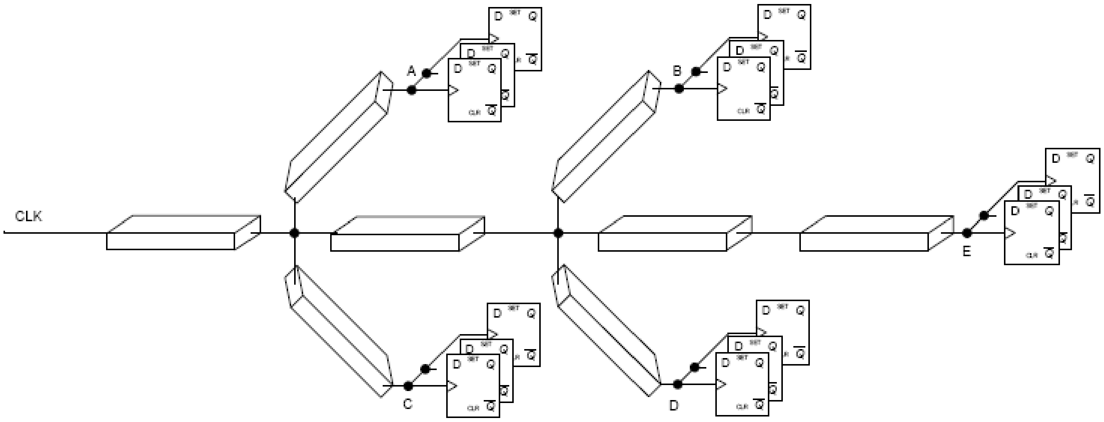


Figure 2: High level diagram of problem 2

The problem can be redrawn as shown in Figure 2a where each component has the following values depending on which wire model is used

Component	**Value**	
	π-model	**simple RC model**
R1 – R8	10 Ohm	10 Ohm
C0	5 fF	0 fF
C1, C3	20 fF	10 fF
C2, C4, C5, C7, C8	305 fF	310 fF
C6	10 fF	10 fF

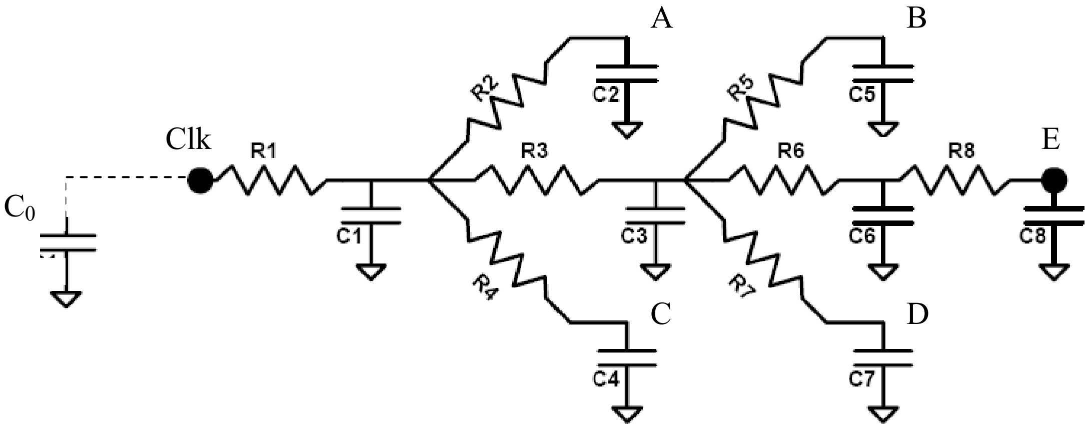


Figure 2a: RC model of problem 2

Obviously the longest delay occurs between the Clk-input and the register E, the shortest one between Clk and A or C.

Using Elmore delay leads to the following results:

$$t_{p,clk-E} = 0.69\,[C_8 \times (R_8 + R_6 + R_3 + R_1) + C_6 \times (R_6 + R_3 + R_1) + (C_5 + C_7) \times (R_3 + R_1) + C_3 \times (R_3 + R_1) + (C_2 + C_4) \times R_1 + C_1 \times R_1]$$

$$t_{p,clk-A} = 0.69\,[(C_1 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) \times R_1 + C_2 \times (R_2 + R_1)] = t_{p,clk-C}$$

$$t_{skew} = t_{p,clk-E} - t_{p,clk-A}$$

When using the π-model this leads to

$t_{p,clk-E} = 21.66$ ps

$t_{p,clk-A} = t_{p,clk-C} = 12.97$ ps

$t_{skew} = 8.74$ ps

When using the regular RC - model this leads to

$t_{p,clk-E} = 21.8$ ps

$t_{p,clk-A} = t_{p,clk-C} = 13.04$ps

$t_{skew} = 8.76$ ps

Problem 3: Transmission Line

A inverter sized up by 50 compared to a minimum sized inverter in our 90 nm technology (remember: Requ is approx. 10kOhm for a minimum sized inverter, you can use this value here) is used to drive a capacitor via a 5 mm long and 1 um wide Aluminum wire. The wire has a sheet resistance of 50 mOhm/um, a capacitance of 50 aF/um^2 and a fringing cap of 40 aF/um. The wire can be approximated as a lossless transmission line and the capacitor at the output can be considered as an open-ended termination for all practical purposes. VDD is equal to 1.2 V for this problem and you can neglect all parasitic capacitances associated with the driving inverter.

a) Determine the propagation delay of the circuit (for the high to low transition at the input). You may assume that the transmission line effect is dominant. Draw the lattice diagram and the Vout waveform during the transition (Vout from VDD to VDD/2)

b) Size up the inverter such that the delay is minimized

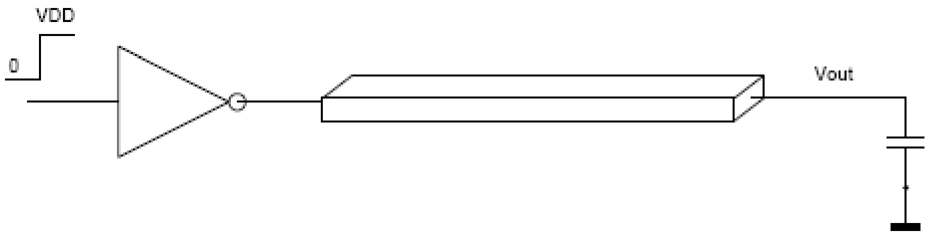


Figure 3: High level diagram of problem 3

a) First, since the inverter is 50 times a minimum inverter its R_{equ} is about 200 Ohm.

Then, the transmission line parameters can be derived as follows (Example 4.4 (p 150) and p 161 in the textbook) :

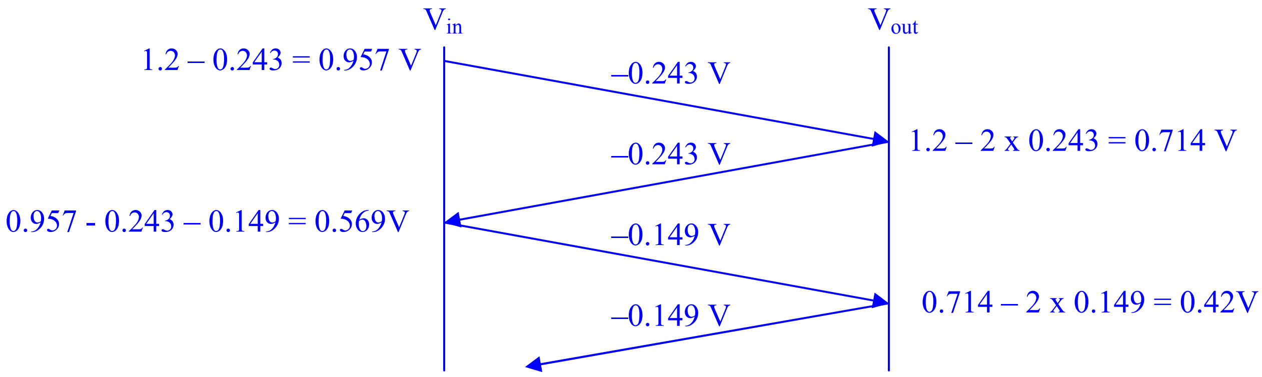
$c = (W \times 50\ aF + 2 \times 40\ aF) = 130\ aF/um$
$l = (\varepsilon_r \times \varepsilon_0 \times \mu_0)/c = (3.9 \times 8.854E\text{-}12 \times 4E\text{-}7 \times \pi)/c = 0.334\ pH/um$
$t_p = sqrt(lc) = 6.59\ fs / um$
$Z_0 = sqrt\ (l/c) = 50.69\ Ohm$
$t_f = t_p \times Length = 6.59\ fs * 5000\ um = 33\ ps$

The low to high transition at the input at the inverter produces a negative step from 1.2 V to 0 as the equivalent voltage source connected to R_s (similar to figure 4.20 in the textbook). The initial voltage levels at the "input" of the transmission line and the output V_{out} are both 1.2 V.

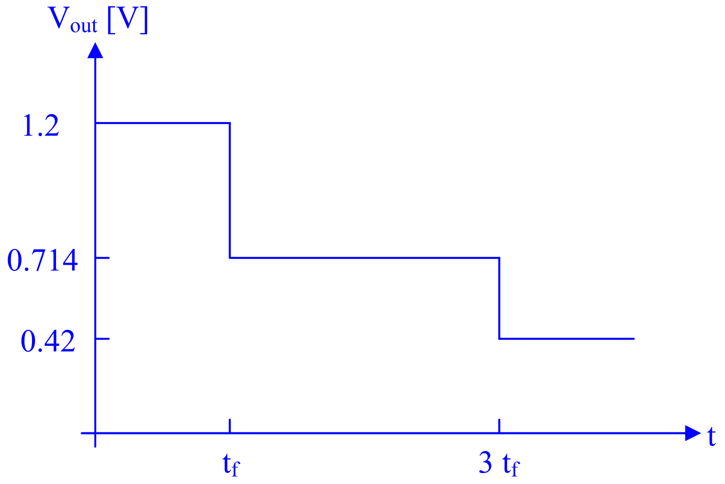
Drive source resistance $R_s = R_{equ} = 200$ Ohm
The initial voltage step at "input" of transmission line:
$-1.2 \times 50.69/(200+50.69) = -0.243$ V
→ $V_{inTML} = 1.2 - 0.243 = 0.957$ V

At the output: $\rho = 1$ (open circuit termination is assumed)
At the inverter output node $\rho_{inv} = (R_s - Z_0)/(R_s + Z_0) = 0.596$

Based on these calculations the following lattice diagram can be drawn



The output transient response looks therefore like:



$t_{pd} = 3\ t_f = 100\text{ps}$

b)

The delay is minimized when the output resistance of the driver is matched to Z_0 which means R_{equ} is approx. 50 Ohm which is the case when the inverter is sized up by another factor of 4 to a total of 200 unit sized inverters.