

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
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Lab #1: Circuit Simulation
Due Friday, February 1st, 5pm, box in 240 Cory
Solutions

EECS 141

1. Plots of Schematics

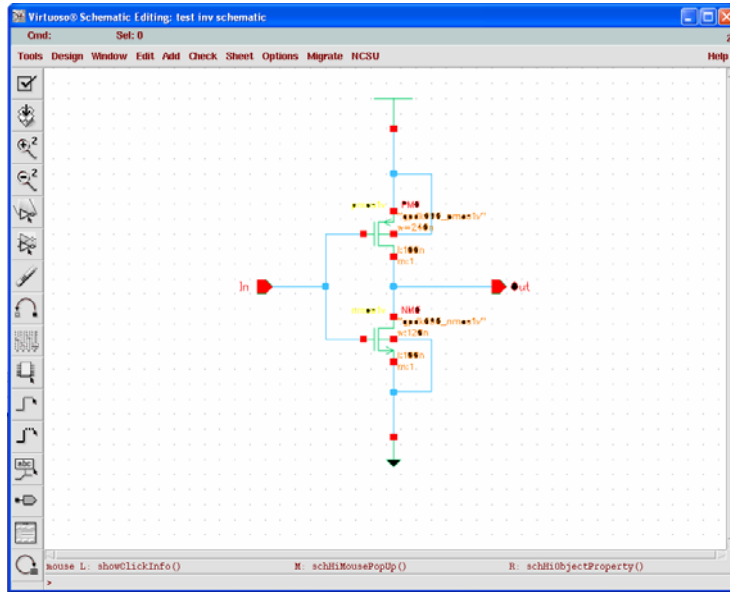


Figure 1: Schematic of Inverter

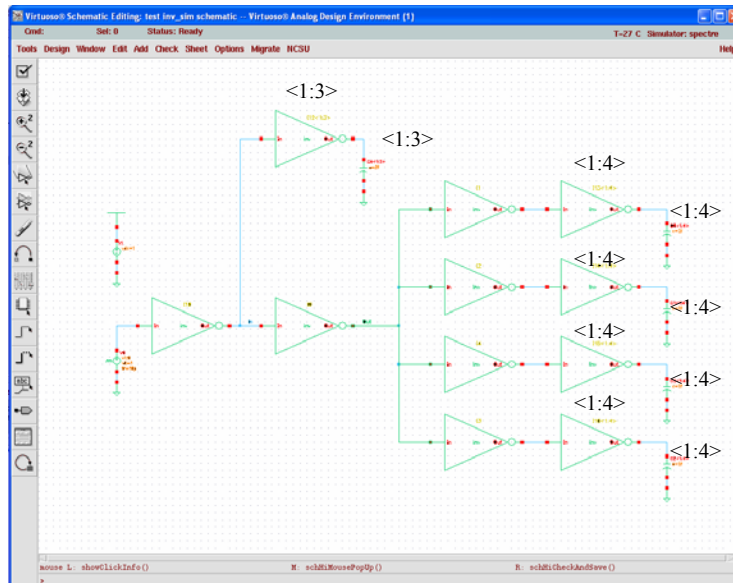


Figure 2: Schematic for Simulation

2. Transient Response of Inverter

The following values for the inverter delays with a loading of 4 identical inverters (= Fan-Out of 4), were obtained from transient simulation.

Delay for rising edge at input: approx. 32.1 ps

Delay for falling edge at input: approx. 39 ps

Figure 3 to 5 show the transient responses of the inverter with different time scaling factors

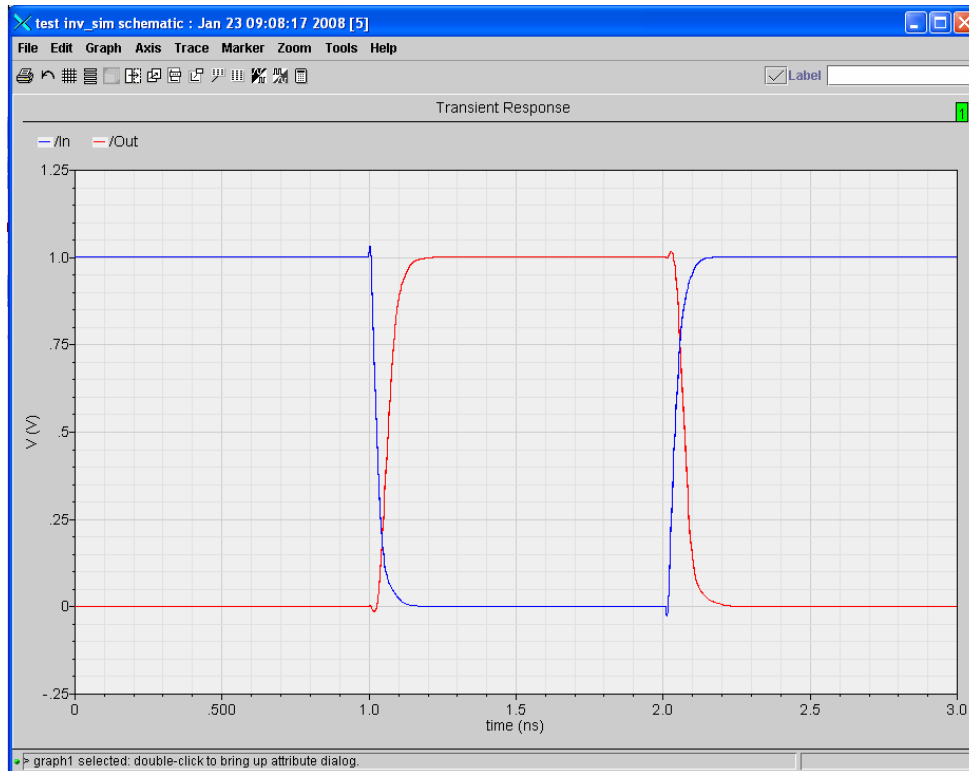


Figure 3: Complete Transient Response of Inverter

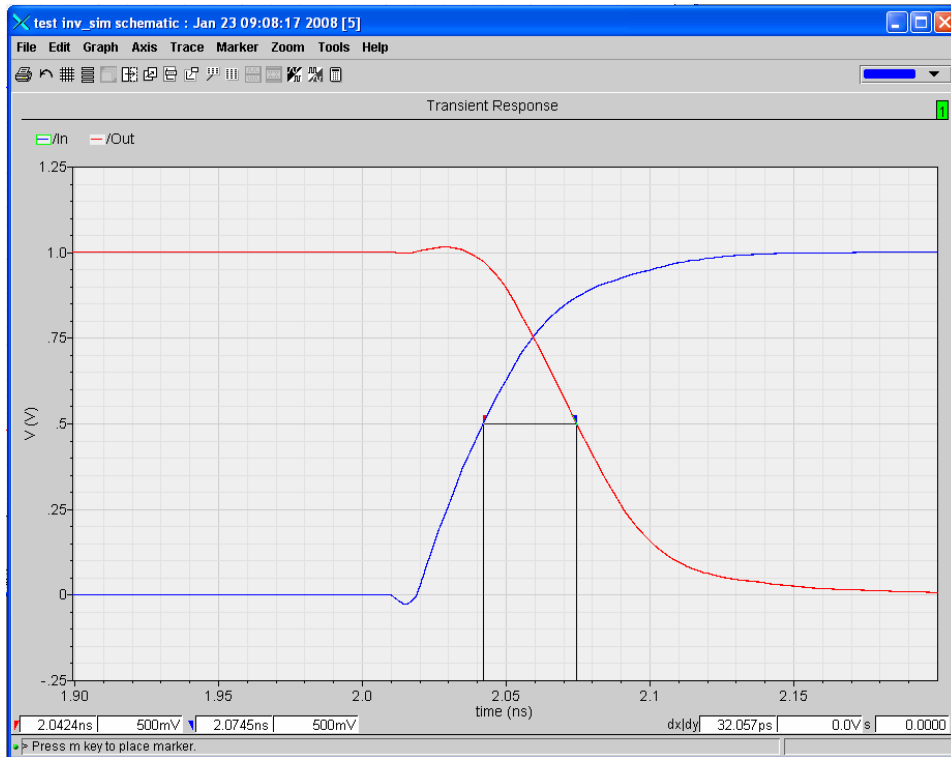


Figure 4: Inverter Delay for Rising Signal Edge at Input

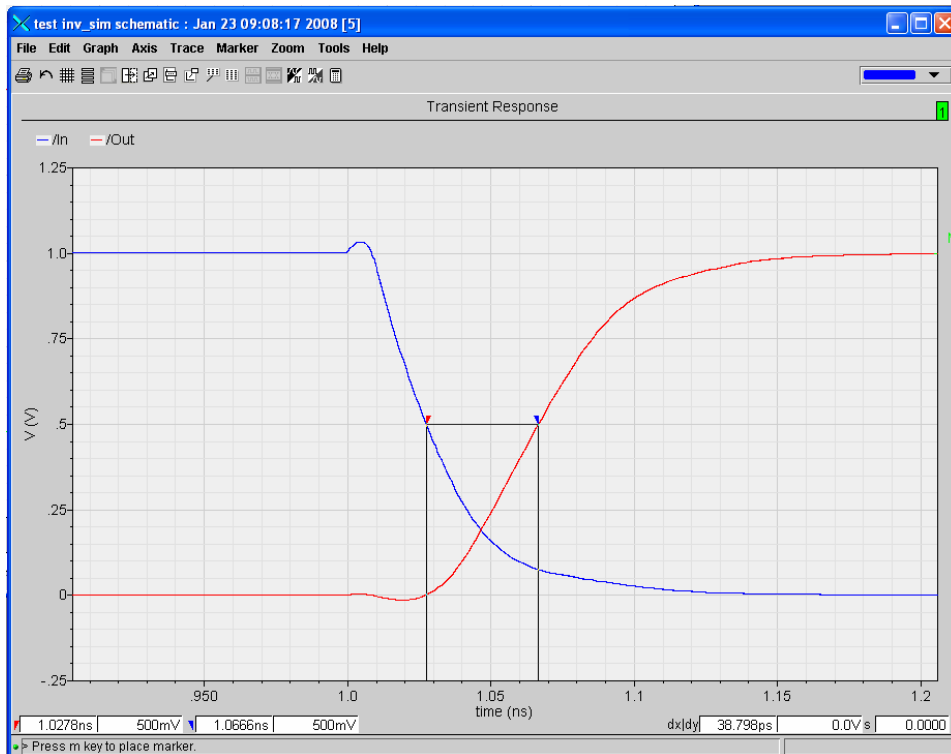


Figure 5: Inverter Delay for Falling Signal Edge at Input

2. Voltage-Transfer Characteristic

Figure 6 shows the simulated VTC of the inverter

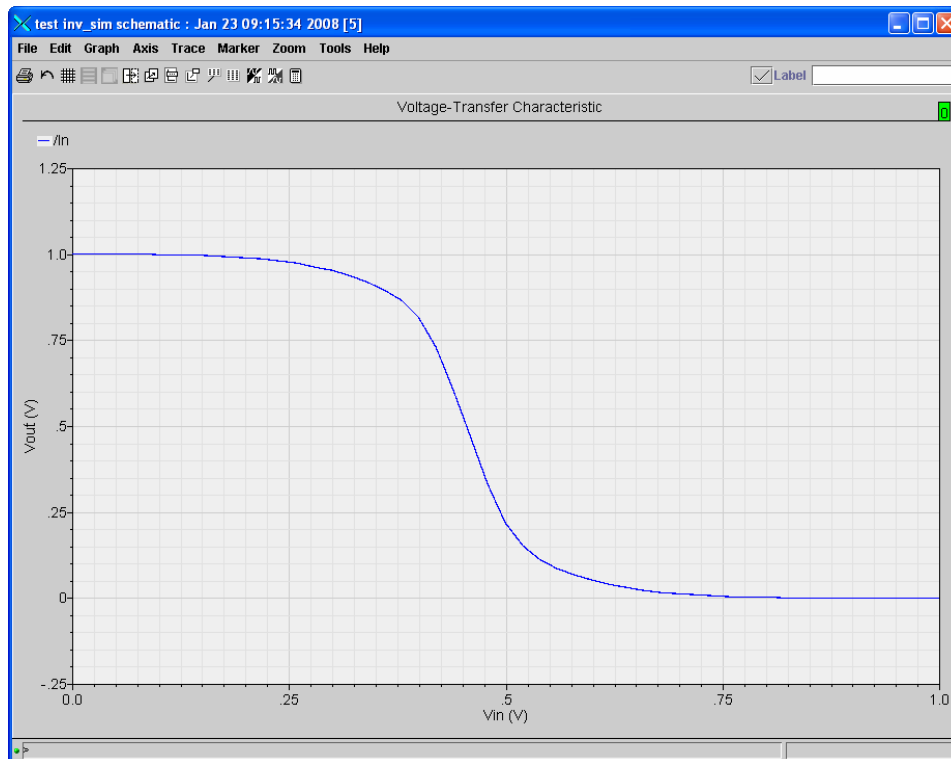


Figure 6: Voltage-Transfer Characteristic of Inverter