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Solution to Homework #3

Problem 1: Unified MOS Transistor Model

1) The simulation results for the NMOS are shown in Figure 1.

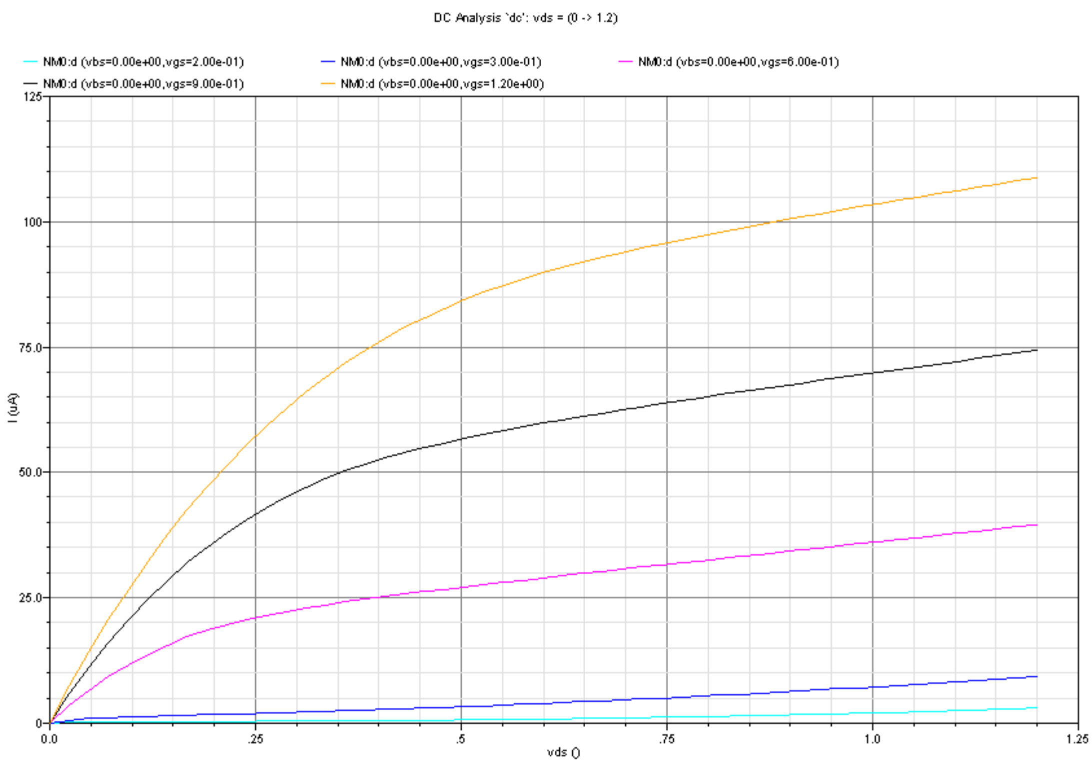

Figure 1: Simulated I_D vs. V_{GS} for the NMOS

There are multiple ways to extract the parameters.
A relatively simple way is to calculate the ratio of two currents of different operating points such that as many terms from the current equation as possible chancel out. Assume your transistor operates in saturation (not velocity saturation!) the expression for the relation of two currents becomes

(1) $$\frac{I_{D1}}{I_{D2}} = \frac{\cancel{k'\frac{W}{2L}}(V_{GS1} - V_{T0})^2 \times (1 + \lambda \times V_{DS1})}{\cancel{k'\frac{W}{2L}}(V_{GS2} - V_{T0})^2 \times (1 + \lambda \times V_{DS2})}$$

If, for example, you pick two currents from curves for different gate-source voltages but at the same value of V_{DS}, the channel length modulation terms chancel out and the only remaining unknown is V_{T0}.
As mentioned before, you have to choose your operating points such that the transistor is in saturation for both of them in order for equation (1) to hold.

For example if you pick V_{GS1} = 0.2 V, V_{GS2} = 0.3 V and V_{DS} = 0.3 you get currents of approx. 0.3 uA and 2.08 uA leading to an extracted **V_{T0} = 0.139 [V]**.

If, at the other hand, you pick two currents with equal values of V_{GS} but different values for V_{DS}, the $V_{GS} - V_{T0}$ terms chancel out and λ remains the only unknown. This time it does not matter whether the transistor is in saturation or in velocity saturation, as long as both operating points are in the same region of operation and it is not operating in the linear region as you can see from equation (2) which relates currents of two operating points in velocity saturation

(2) $$\frac{I_{D1}}{I_{D2}} = \frac{\cancel{k'\frac{W}{L}}\left[(V_{GS1} - V_{T0}) \times V_{VSAT} - \frac{V_{VSAT}^2}{2}\right] \times (1 + \lambda \times V_{DS1})}{\cancel{k'\frac{W}{L}}\left[(V_{GS2} - V_{T0}) \times V_{VSAT} - \frac{V_{VSAT}^2}{2}\right] \times (1 + \lambda \times V_{DS2})}$$

For example if you pick V_{GS} = 0.9 V, V_{DS1} = 0.6 V and V_{DS2} = 1.2 V you get currents of approx. 59.7 uA and 74.26 uA leading to an extracted **λ = 0.534 [1/V]**.

You can now go ahead and extract k' by picking a current at an operating point in saturation and simple solve the equation for that region of operation (equation (3)) for k'.

(3) $$I_D = k'\frac{W}{2L}(V_{GS1} - V_{T0})^2 \times (1 + \lambda \times V_{DS1})$$

Doing so at V_{GS} = 0.3 and V_{DS} = 0.5 leads to **k' = 162 [uA/V^2]**

Now that almost everything is known, you can pick an operating point in velocity saturation and solve for V_{VSAT} in equation (4)

(4) $$I_D = k'\frac{W}{L}\left[(V_{GS} - V_{T0}) \times V_{VSAT} - \frac{V_{VSAT}^2}{2}\right] \times (1 + \lambda \times V_{DS})$$

One point where the transistor is definitely in velocity saturation is at $V_{GS} = V_{DS} = V_{DD} = 1.2$ V. The current there is approx. 108.7 uA and solving for V_{VSAT} leads to **$V_{VSAT} = 0.395$ [V]**

2) Figure 1 shows a comparison between the simulation results and the unified MOS model using the parameters extracted above. You can see that we actually did a fairly decent job in part 1.

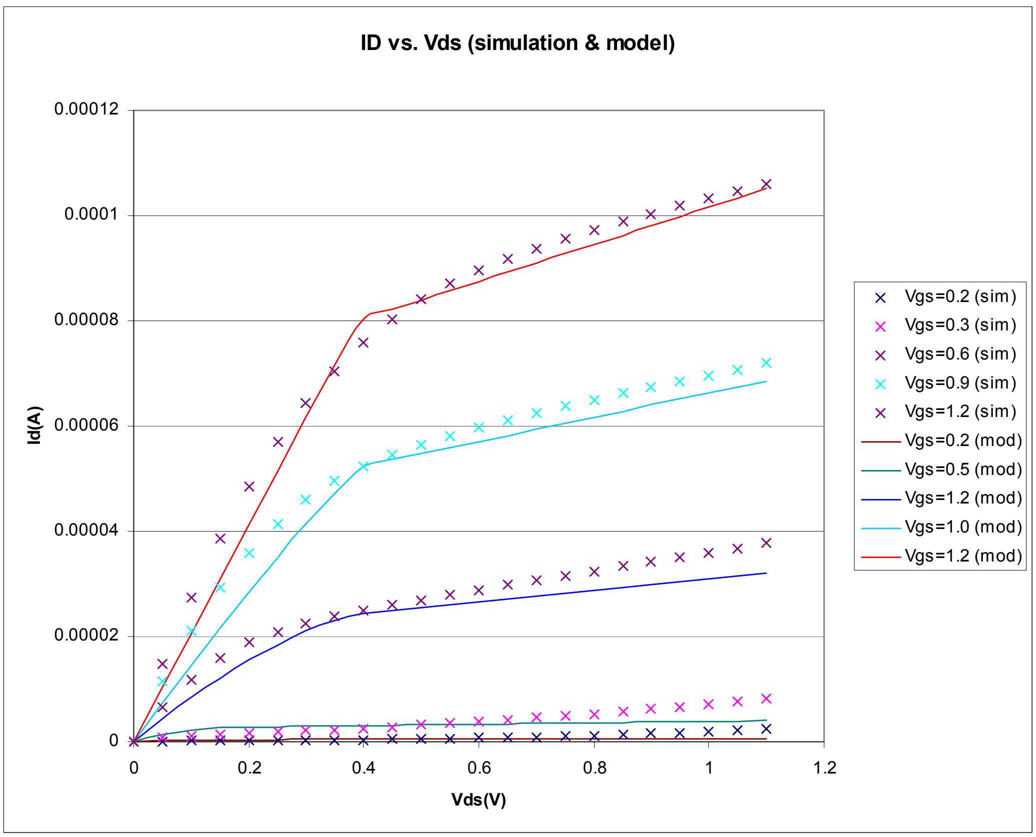

Figure 2: Comparison between simulation and the unified MOS model using the parameters extracted in part 1)

However, we slightly underestimated the currents and we can tweak for it to obtain a better match, especially for high values of V_{GS} and V_{DS} since these are the regions in which the transistor is operating when discharging the load capacitance. Increasing k' by 15 %, decreasing V_{VSAT} by the same amount and increasing V_{T0} by 10 % is sufficient to get a better match as can be seen in Fig 2.

The final parameters are therefore **k' = 190 uA/V^2, λ = 0.535 1/V, V_{T0} = 0.153 V** and **V_{VSAT} = 0.336 V**

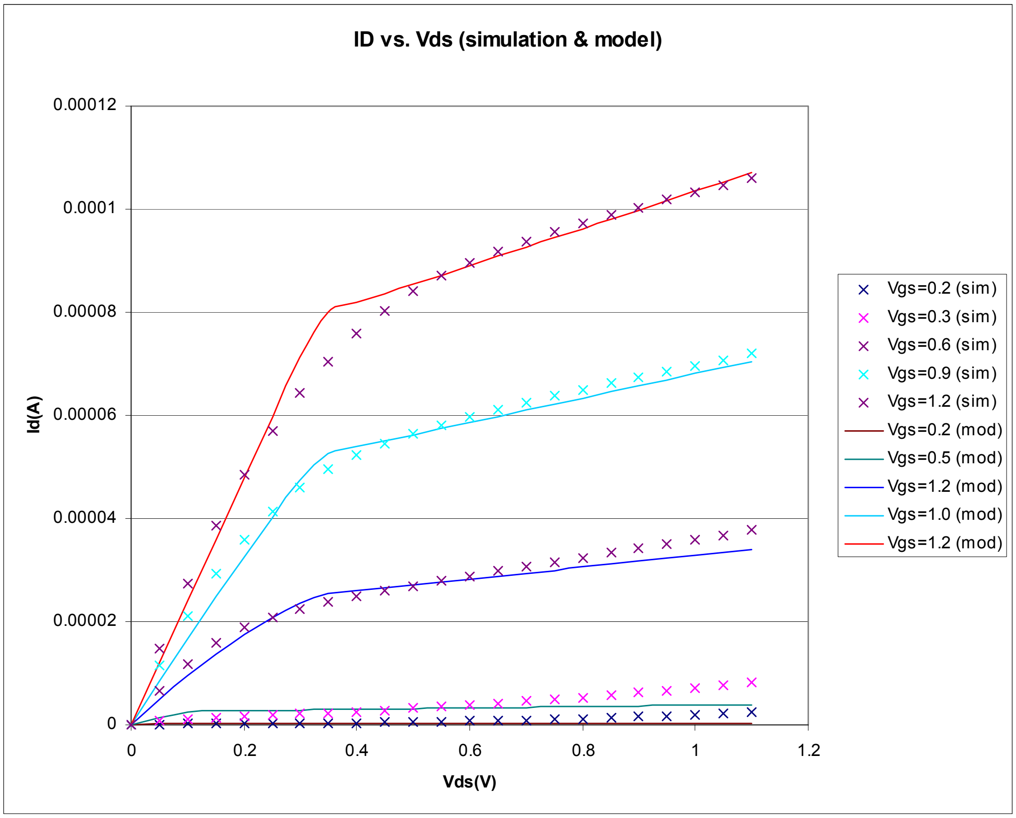

Figure 3: Comparison between simulation and the unified MOS model with modified parameters for the NMOS

3) Figure 4 shows the simulation results for the PMOS. Note that I_D is plotted versus the absolute value of V_{GS}.

   Carrying out the same steps as in 1) leads to the following results for the PMOS parameter:

   V_{T0}: V_{GS1} = 0.2 V, V_{GS2} = 0.3 V and V_{DS} = 0.3 → **V_{T0} = 0.162 [V]**

   λ: V_{GS} = 0.9 V, V_{DS1} = 0.6 V and V_{DS2} = 1.2 V → **λ = 0.5 [1/V]**

   k': V_{GS} = 0.4 and V_{DS} = 0.5 → **k'= 49.15 [uA/V^2]**

   V_{VSAT}: V_{GS} = V_{DS} = V_{DD} = 1.2 V → **V_{VSAT} = 0.78 [V]**

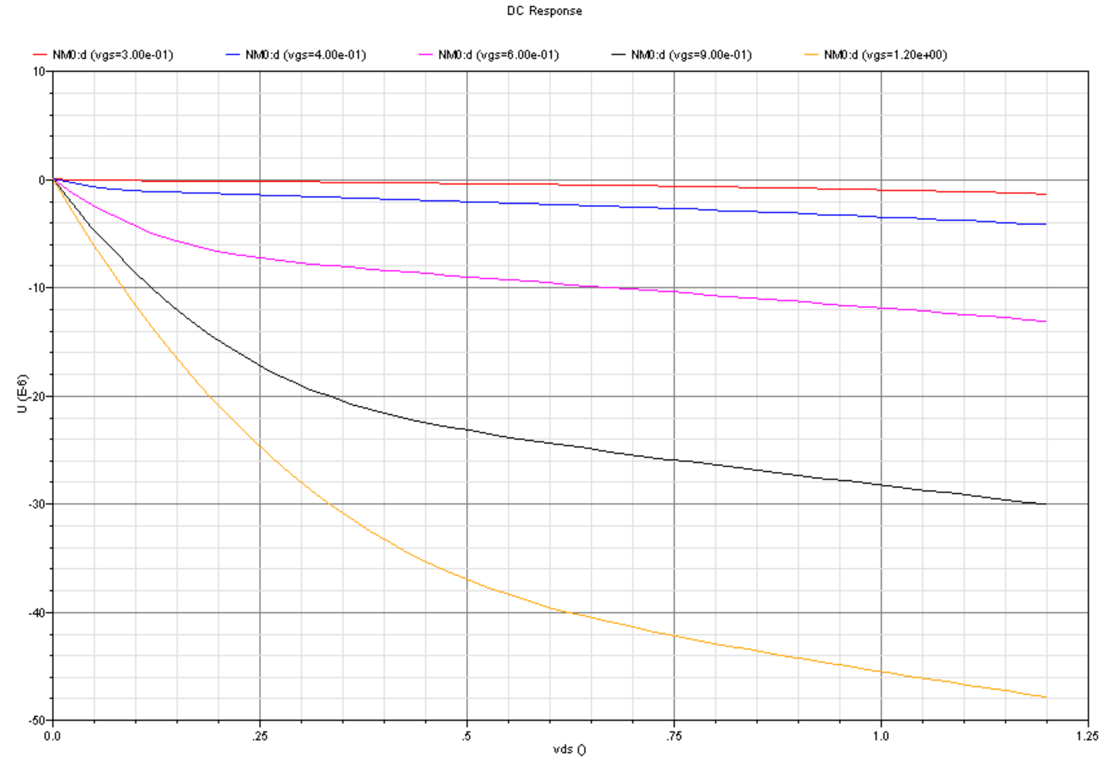

Figure 4: Simulated I_D vs. $|V_{GS|}$ for the PMOS

Bonus: Comparison Simulation - Model

Figure 5 shows the comparison of the simulation with the unified model using the parameters for the PMOS extracted above. This time the match is not nearly as nice as for the NMOS. However, the region in which we are most interested when estimating delays (high V_{DS} and V_{GS}) matches fairly well again.
Tweaking the extracted values by a bit (increasing k' by 60 %, decreasing V_{VSAT} by 50% amount and increasing V_{T0} by 10 %) leads to a much better match between simulation and model, as shown in Figure 6. The final parameters used in Figure 6 are therefore **k' = 78.6 uA/V^2, λ = 0.5 1/V, V_{T0} = 0.1782 V** and **V_{VSAT} = 0.39 V**

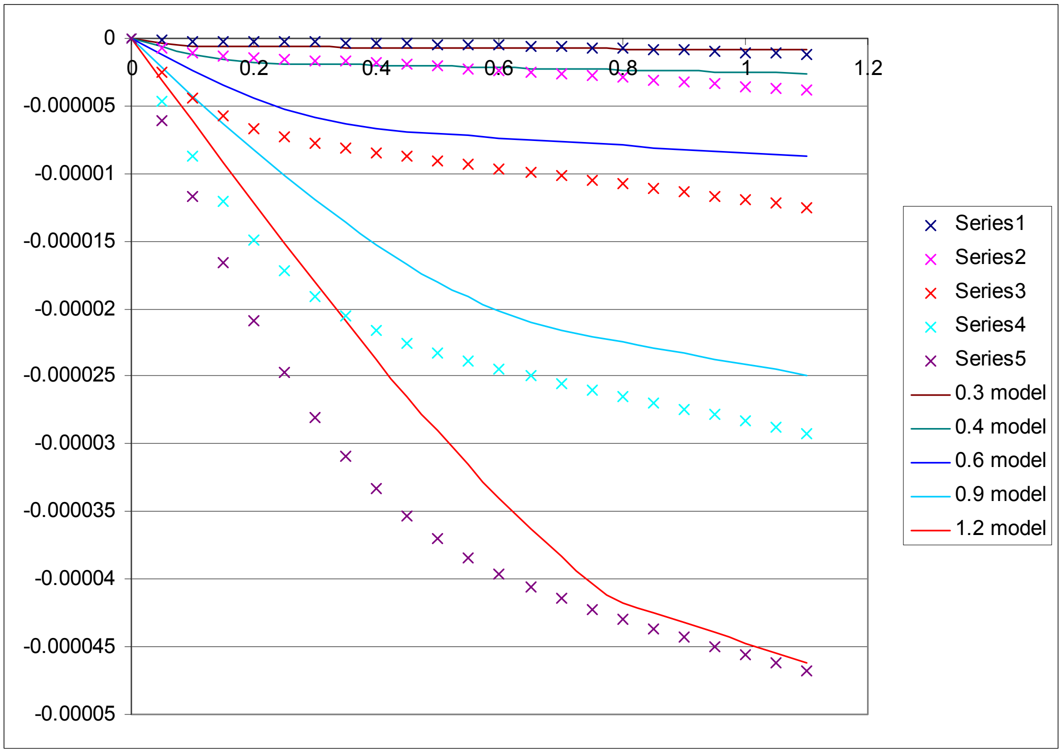

Figure 5: Comparison between simulation and the unified MOS model using the parameters extracted from simulation for the PMOS

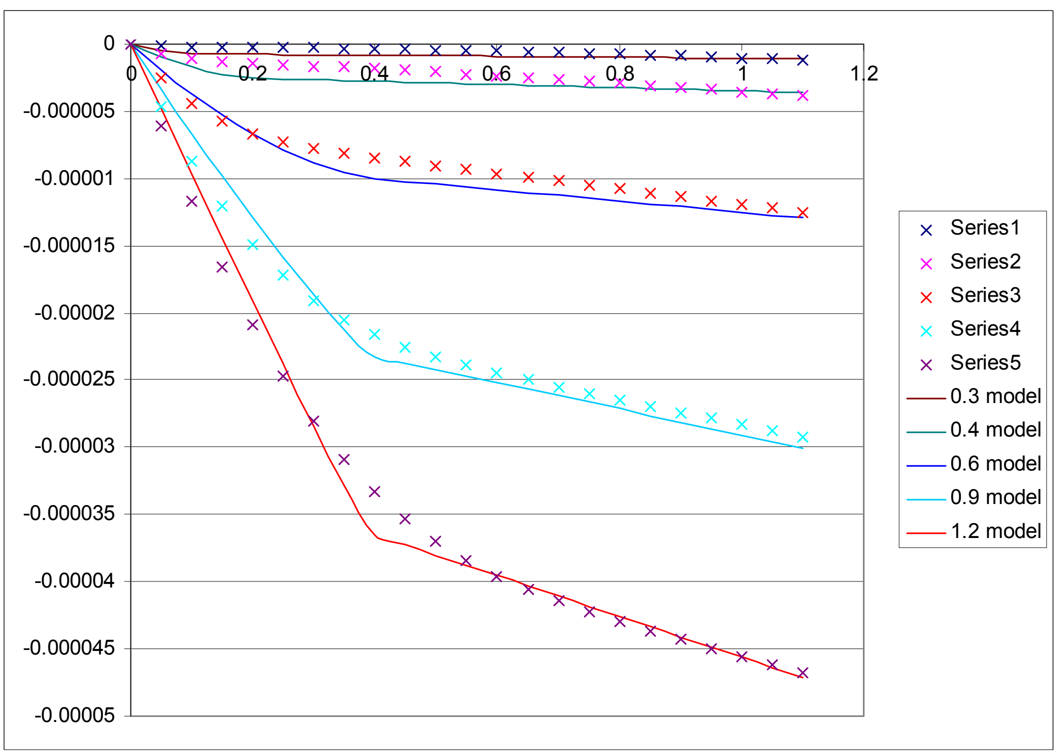

Figure 6: Comparison between simulation and the unified MOS model with modified parameters for the PMOS

Problem 2: VTC

1) A low input signal leads to the transistor being turned off and the output gets pulled to V_{DD} via the resistor R. When a signal higher than V_{T0} is applied to the input signals the transistor starts turning on and the output voltage gets pulled towards gnd. Therefore the shown circuit acts behaves like an inverter. The major drawbacks of a structure like this are e.g. a static current when the input is high and a degraded output low level (V_{OL} not equal to gnd).

2) Since the NMOS transistor is turned off when a low input signal is applied, the inverter pulls the output up all the way to V_{DD} and making **V_{OH} equal to V_{DD}**. When a high input signal (V_{DD}) is applied to the input, the NMOS is turned on and the output voltage can be calculated by equating the currents through R and through the transistor. In order to apply the correct equation for the NMOS, one has to start by assuming a region of operation for the transistor. Since the output voltage is likely to be rather low and $V_{GS} - V_T$ is rather high, we start by assuming that the transistor is operating in the linear region. Equating the currents leads to the following equation.

(5) $$\frac{V_{DD} - V_{OL}}{R} = k'\frac{W}{L}\left[(V_{DD} - V_T)V_{OL} - \frac{V_{OL}^2}{2}\right] \times (1 + \lambda \times V_{OL})$$

Plugging in all the values obtained from Problem 1 (assuming they do not change for different values of W) as well as W/L = 6 and solving for V_{OL} leads to a **V_{OL} of approx. 92.5 mV.** Since V_{OL} is at the same time the V_{DS} of our transistor it is clear that the transistor is operating in the linear region and that we derived a valid solution.
V_M can be calculated in a similar way by using the definition of V_M being the voltage where V_{IN} equals V_{OUT}. It is a reasonable guess to assume V_M being somewhere around V_{DD} / 2 and therefore the transistor operating in velocity saturation. V_M can therefore be found by again equating the currents through R and the NMOS in velocity saturation and by setting $V_{IN} = V_{OUT} = V_M$. Doing so leads to equation (6)

(6) $$\frac{V_{DD} - V_M}{R} = k'\frac{W}{L}\left[(V_M - V_T)V_{VSAT} - \frac{V_{VSAT}^2}{2}\right] \times (1 + \lambda \times V_M)$$

and a **V_M of approx. 473 mV** which means that the transistor is indeed in velocity saturation - our assumption and our solution was therefore correct.

3) An NMOS-only inverter can e.g. be build by replacing the resistor of the inverter in Fig. 4 of the homework with an NMOS with its gate connected to

its drain, which is connected to V_{DD} (such a transistor is said to be diode-connected, since it basically acts like a diode)). When the input is high, both transistors try to drive the outputs in different directions. Since for a high input, the output should be closer to gnd than to V_{DD}, the bigger (wider) NMOS transistor is placed on the bottom, whereas the minimum NMOS is used to replace the resistor. In order to reduce the voltage drop across the top NMOS during the input low state, the bulk of the top NMOS is connected to its source (which is connected to the output node of the inverter). Doing so also simplifies the analysis required in the next step a bit since the body effect can be neglected. The resulting inverter schematic is shown in Figure 7.

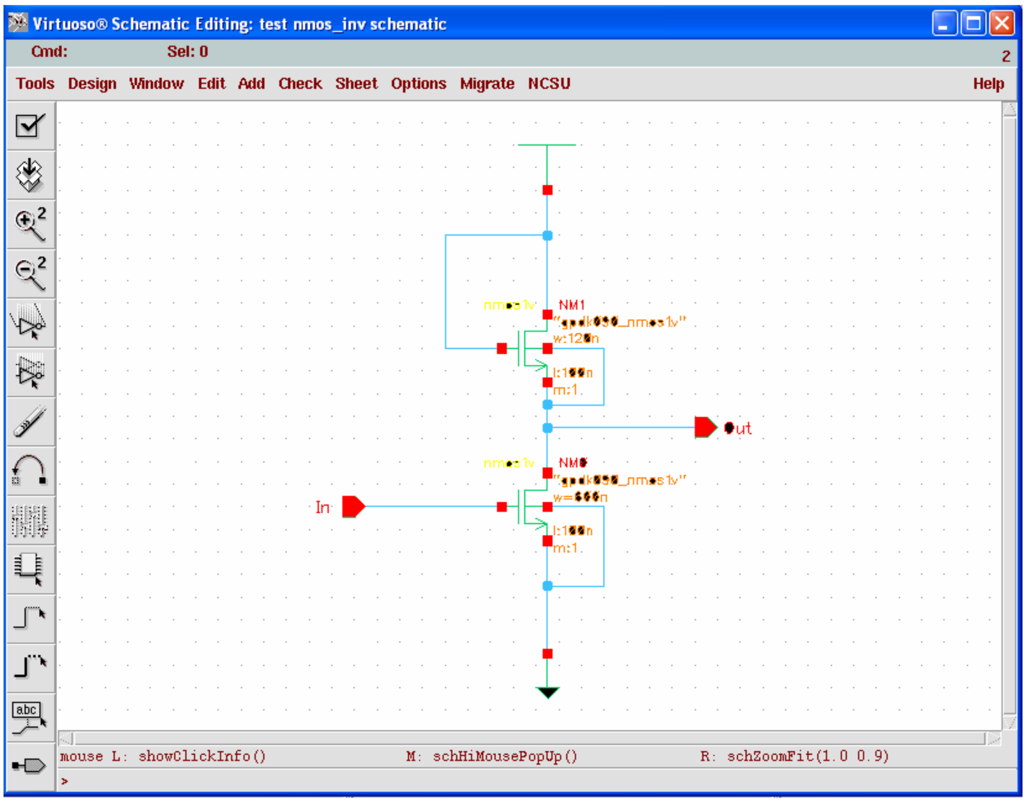

Figure 7. Schematic of an NMOS-only inverter.

4) For low input voltages the top NMOS transistor pulls the output towards V_{DD}. However, since the voltage between gate and source has to be always larger than V_{DD} for the NMOS to be on, there is always a voltage drop of at least approx. V_T across this transistor. This simple observation leads to an estimate for $\mathbf{V_{OH}}$ of $V_{DD} - V_T$ which **is approx. 1.047 V.** V_{OL} can be calculated by equating currents again, similar as was done in the inverter with resistor case. Assuming that V_{OL} will be rather low, assuming that the top transistor will operate in velocity saturation and the bottom transistor will operate in the linear region is a reasonable starting point. Also, for our hand calculations we assume that the transistor parameters derived in Problem 1 don't change with W.

(Note: Throughout this problem we are using the fitted parameters for the unified MOS model obtained in Problem 1)
All this leads to the following expression

(7)
$$k'\frac{W}{L}\left[(V_{DD}-V_{OL}-V_T)V_{VSAT}-\frac{V_{VSAT}^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_{OL})) = k'\frac{5W}{L}\left[(V_{DD}-V_T)V_{OL}-\frac{V_{OL}^2}{2}\right]\times(1+\lambda\times V_{OL})$$

which can be solved for $\mathbf{V_{OL}}$ leading to a value of **approx. 81.6 mV**. This value of V_{OL} validates the assumptions of the regions of operations for the transistors we made. For calculating V_M we start again by assuming that both transistors are operating in velocity saturation and replace V_{OL} and V_{IN} by $V_{M.}$ This allows us to write down the following equation

(8)
$$k'\frac{W}{L}\left[(V_{DD}-V_M-V_T)V_{VSAT}-\frac{V_{VSAT}^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_M)) = k'\frac{5W}{L}\left[(V_M-V_T)V_{VSAT}-\frac{V_{SAT}^2}{2}\right]\times(1+\lambda\times V_M)$$

Solving equation (8) for V_M gives a value of 0.45 V. However, the bottom NMOS transistor biased with a V_{GS} would technically operate in saturation rather than in velocity saturation (although only by a bit). Therefore equation (8) needs to be modified such that the larger NMOS now operates in saturation, which leads to

(9)
$$k'\frac{W}{L}\left[(V_{DD}-V_M-V_T)V_{VSAT}-\frac{V_{VSAT}^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_M)) = k'\frac{5W}{L}\times\frac{(V_M-V_T)^2}{2}\times(1+\lambda\times V_M)$$

The new result for $\mathbf{V_M}$ is now **0.42 V** which is only slightly lower than the result obtained previously.
In order to calculate the gain of the VTC at V_M we first rewrite equ. (9) in terms of V_{in} and V_{out}. This leads to

(10)
$$k'\frac{W}{L}\left[(V_{DD}-V_{out}-V_T)V_{VSAT}-\frac{V_{VSAT}^2}{2}\right]\times(1+\lambda\times(V_{DD}-V_{out})) = k'\frac{5W}{L}\times\frac{(V_{in}-V_T)^2}{2}\times(1+\lambda\times V_{out})$$

Next, we solve equ (10) for V_{out} which ends up being a function of V_{in}.

$$V_{out} = f(V_{in}) \quad (11)$$

Since g, the gain of the VTC, is nothing else then $\Delta V_{out} / \Delta V_{in}$ at $V_{in} = V_M$ it can be derived by building the derivative of V_{out} with respect to V_{in} ($\delta V_{out} / \delta V_{in}$) and calculating the numerical result at $V_{in} = V_M$. Doing so leads to a **g of -2.5**.

V_{IL} and V_{IH} can now be calculated by calculating the intersecting points of the straight line going trough V_M with a slope of g and V_{OH} and V_{OL} respectively. This leads to **V_{IL} = 0.17 V and V_{IH} = 0.56 V.**

5) Figure 8 shows the comparison between the simulated (blue) and the VTC obtained by hand calculations (red) and Figure 9 shows the simulated slope of the VTC (with the markers placed at points where the slope equals -1). The two results match pretty well, which indicates that we did a pretty good job on the parameter extraction

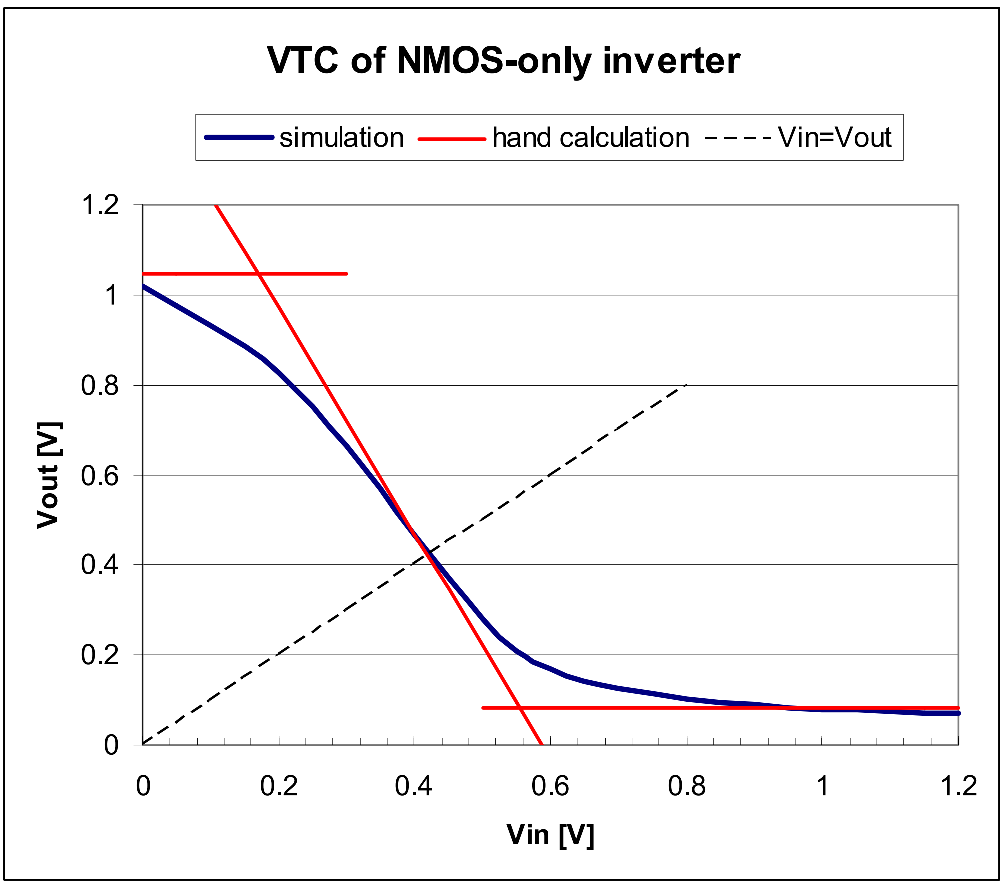

Figure 8. Comparison of simulated and estimated VTC of NMOS only inverter

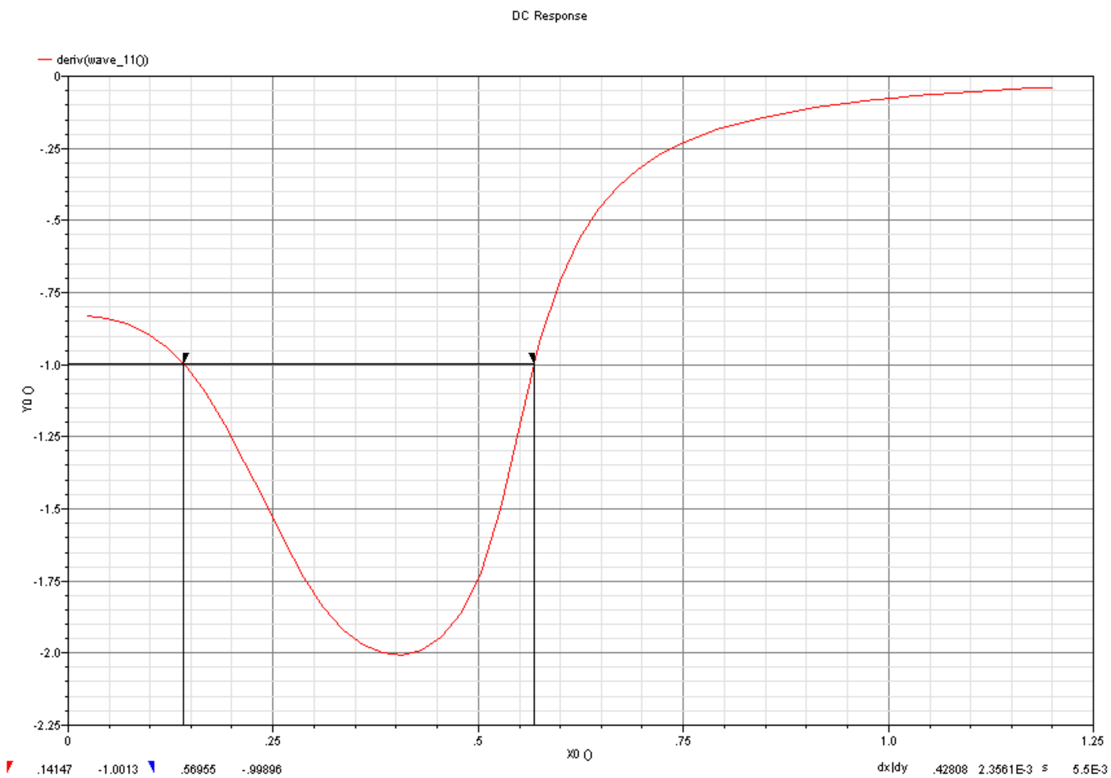

Figure 9. Simulated slope of the VTC of the NMOS only inverter

6) Some problems of a logic based only on NMOS transistors are:

- Static current when input high
- Output low bigger than 0, output high lower than V_{DD} (no rail to rail output, → reduced noise margin)
- Lower gain at V_M
- size

Problem 3: Inverter Delay Estimation

1) The various components of the equivalent C_L can be calculated as indicated in Table 5.2 of the textbook.

   The non-junction related components can be calculated rather straight forward:

   $C_{gdn} = 2 * W_n * C_{gdon} = 0.091$ fF
   $C_{gdp} = 2 * W_p * C_{gdop} = 0.17$ fF
   $C_{gn} = (C_{gdon} + C_{gson})W_n + C_{ox} * W_n * L_n = 0.268$ fF
   $C_{gp} = (C_{gdop} + C_{gsop})W_p + C_{ox} * W_p * L_p = 0.526$ fF

   For the capacitances related to the drain/source to substrate junctions however, we need to calculate a K_{eq} for the transitions to be able to treat these capacitances as linear ones (5.4.1 textbook). K_{eq} can be calculated by the following equation

$$K_{eq} = \frac{-\phi_0{}^m}{(V_{high} - V_{low})(1-m)}\left[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}\right] \tag{12}$$

(Note that V_{high} and V_{low} are negative voltages since they are reverse voltages across the junctions)

Assuming the inverter switches at $V_{DD}/2$ the following values for K_{eq} can be calculated:

$$K_{eqn,h\to l} = \frac{-0.9^{0.222}}{(-1.2+0.6)(1-0.222)}\left[(0.9+1.2)^{1-0.222} - (0.9+0.6)^{1-0.222}\right] = 0.86$$
$$K_{eqn,l\to h} = \frac{-0.9^{0.222}}{(-0.6)(1-0.222)}\left[(0.9+0.6)^{1-0.222} - (0.9)^{1-0.222}\right] = 0.94$$
$$K_{eqswn,h\to l} = \frac{-0.9^{0.01}}{(-1.2+0.6)(1-0.01)}\left[(0.9+1.2)^{1-0.01} - (0.9+0.6)^{1-0.01}\right] = 0.993$$
$$K_{eqswn,l\to h} = \frac{-0.9^{0.01}}{(-0.6)(1-0.01)}\left[(0.9+0.6)^{1-0.01} - (0.9)^{1-0.01}\right] = 0.997$$
$$K_{eqp,h\to l} = \frac{-0.9^{0.331}}{(-1.2+0.6)(1-0.331)}\left[(0.9+1.2)^{1-0.331} - (0.9+0.6)^{1-0.331}\right] = 0.8$$
$$K_{eqp,l\to h} = \frac{-0.9^{0.331}}{(-0.6)(1-0.331)}\left[(0.9+0.6)^{1-0.331} - (0.9)^{1-0.331}\right] = 0.91$$
$$K_{eqswp,h\to l} = K_{eqswn,h\to l} = 0.993$$
$$K_{eqswp,l\to h} = K_{eqswn,l\to h} = 0.997$$

The drain and source geometries can be obtained from the properties window in cadence. Their values are as follows:

AD_n = 69.7 f
AD_p = 69.7 f
PD_n = 1.16 u
PD_p = 1.04 u

Once all these values are known the equivalent capacitances can be calculated.

$C_{dbn,l\to h} = K_{equn,l\to h} * AD_n * C_{jon} + K_{eqswn,l\to h} * PD_n * C_{jswon}$ = 0.11 fF
$C_{dbn,h\to l} = K_{equn,h\to l} * AD_n * C_{jon} + K_{eqswn,h\to l} * PD_n * C_{jswon}$ = 0.1 fF
$C_{dbp,l\to h} = K_{equp,l\to h} * AD_p * C_{jop} + K_{eqswp,l\to h} * PD_p * C_{jswop}$ = 0.1 fF
$C_{dbp,h\to l} = K_{equp,h\to l} * AD_p * C_{jop} + K_{eqswp,h\to l} * PD_p * C_{jswop}$ = 0.094 fF

The total equivalent FO4 - C_Ls for each transition are therefore

$C_{L,l\rightarrow h} = C_{gdn} + C_{dgp} + C_{dbn,l\rightarrow h} + C_{dbp,l\rightarrow h} + 4(C_{gn} + C_{gd}) = 3.647$ fF
$C_{L,h\rightarrow l} = C_{gdn} + C_{dgp} + C_{dbn,h\rightarrow l} + C_{dbl,h\rightarrow l} + 4(C_{gn} + C_{gd}) = 3.631$ fF

2) The equivalent resistance of a transistor over the range of interest ($V_{DS} = V_{DD}/2 \rightarrow V_{DD}$) can be calculated by

$$(13)\quad R_{eq} = average_{t=t1\ldots t2}(R_{on}(t)) = \frac{1}{t_2 - t_1}\int_{t1}^{t2} R_{on}(t)dt = \frac{1}{t_2 - t_1}\int_{t1}^{t2} \frac{V_{DS}(t)}{I_D(t)}dt$$

as shown on p104 ff in the textbook.

Solving equ. 13 leads to

$$(14)\qquad R_{eq} \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

where

$$(15)\qquad I_{DSAT} = k'\frac{W}{L}\left((V_{DD} - V_T)V_{vsat} - \frac{V_{vsat}^2}{2}\right)$$

Plugging in the values obtained in part 1 of this homework into equations (14) and (15) leads to an R_{eqn} of 8.3 kΩ for the NMOS and an R_{eqp} of 10.3 kΩ.

3) Based on the results from 1) and 2) the delay of the inverter is estimated to be

$$\tau_{D,;\rightarrow h} = 0.69 \times C_{L,l\rightarrow h} \times R_{eqp} \approx 26ps$$
$$\tau_{D,h\rightarrow l} = 0.69 \times C_{L,h\rightarrow l} \times R_{eqn} \approx 20.8ps$$
$$\tau_D = \frac{\tau_{D,l\rightarrow h} + \tau_{D,h\rightarrow l}}{2} \approx 23.4ps$$

4) Figures 10 and 11 show the simulated FO4 delay. The values for the low-to-high and high-to-low delays are approximately 26.3 ps and 22.6 ps which is fairly close to the estimated values. The remaining mismatch is due to various reasons: Some obvious ones are the simplifications in the capacitor as well as in the equivalent resistor models (p197 and 104 in the textbook) and the inaccuracies related to the extraction of the parameters of the unified model. Another reason for the mismatch is that at the beginning of the switching cycle both transistors are actually on (since the input signal is not an ideal step function) and work against each other, slowing down the transition.

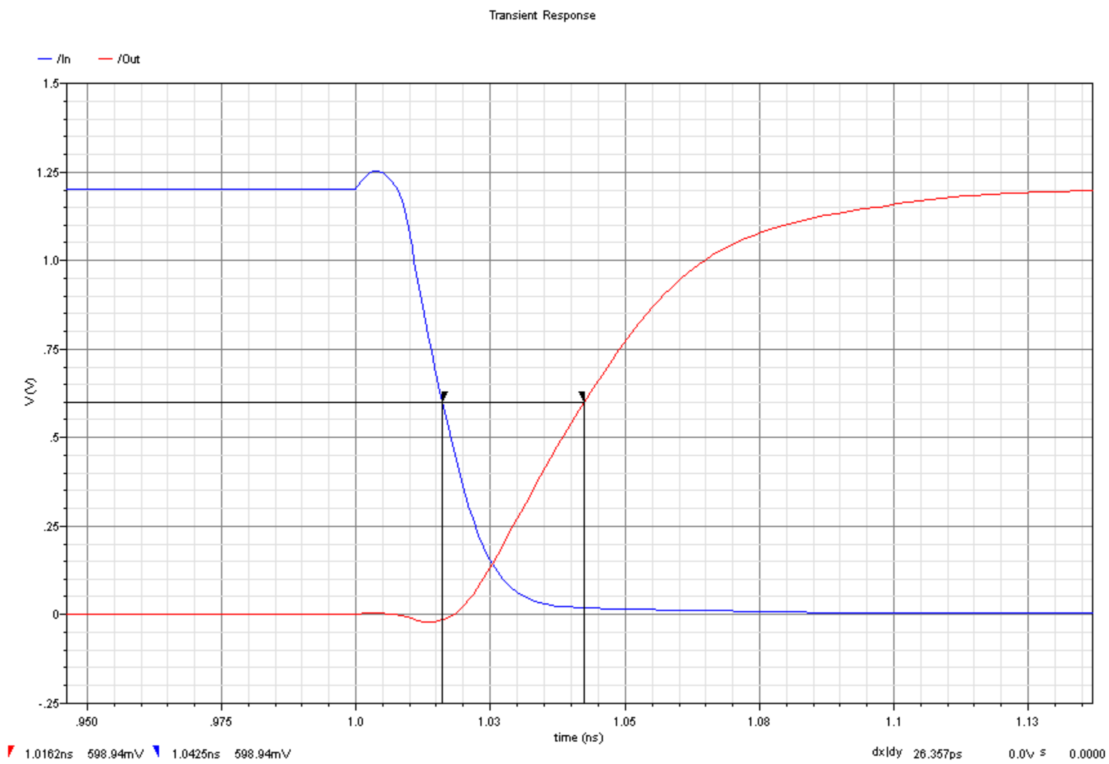

Figure 10. Simulated low-to-high FO4 delay

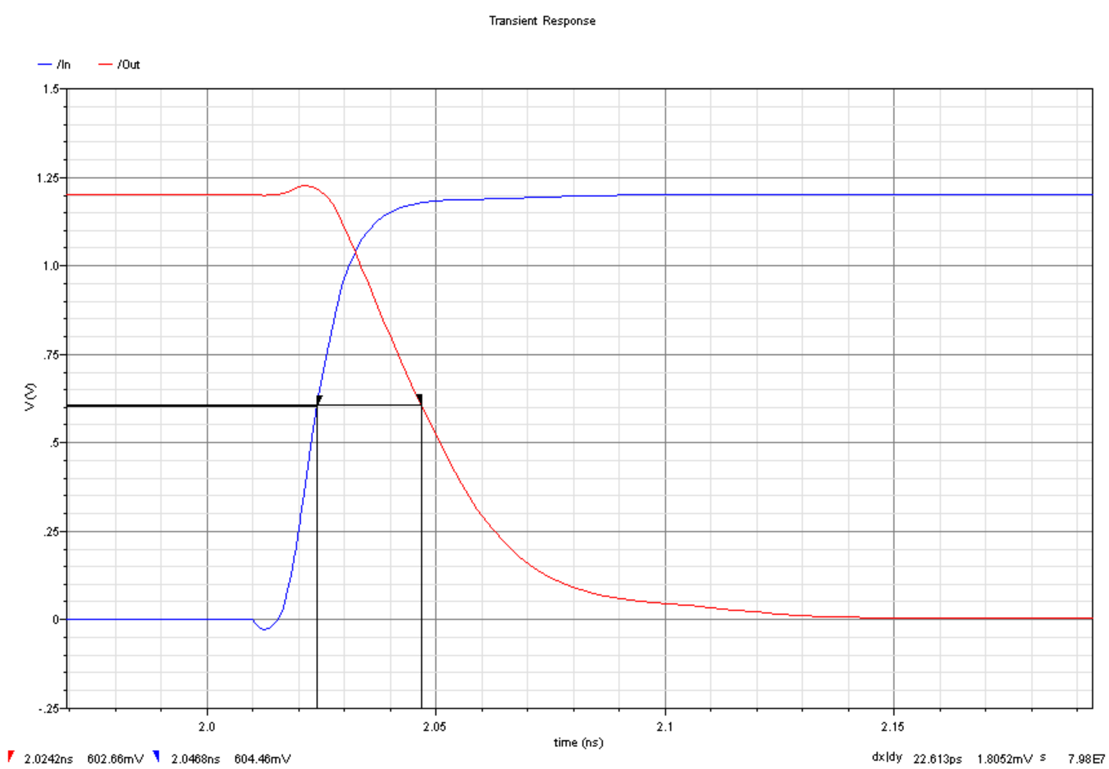

Figure 11. Simulated high-to-low FO4 delay