

EE141-Spring 2008

Digital Integrated Circuits

Lecture 12
CMOS Logic-speed

Announcements

- Lab5 this week
- Midterm results next We



CMOS Logic

Review

□ Last lecture:

- CMOS Logic
- Standard cell design

□ This lecture

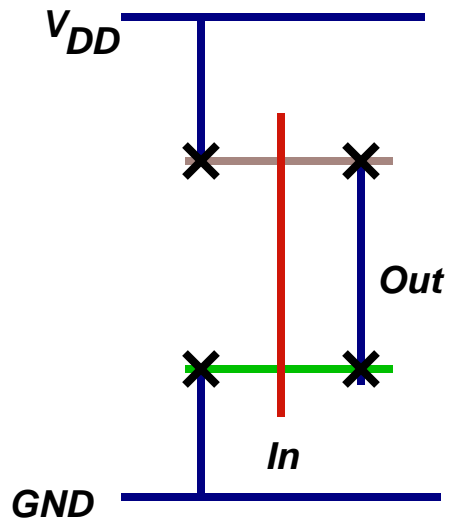
- Performance optimization in CMOS logic

Stick Diagrams

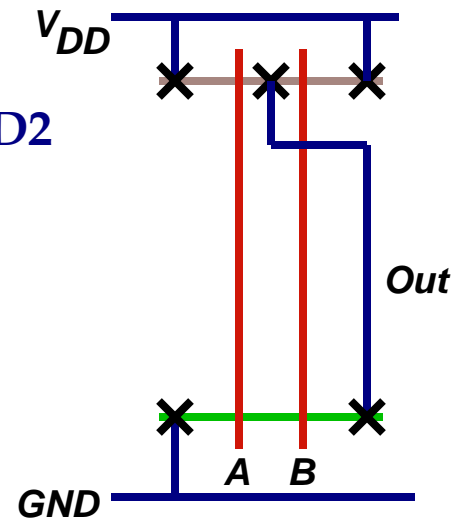
Contains no dimensions

Represents relative positions of transistors

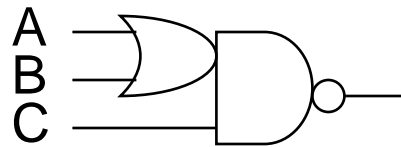
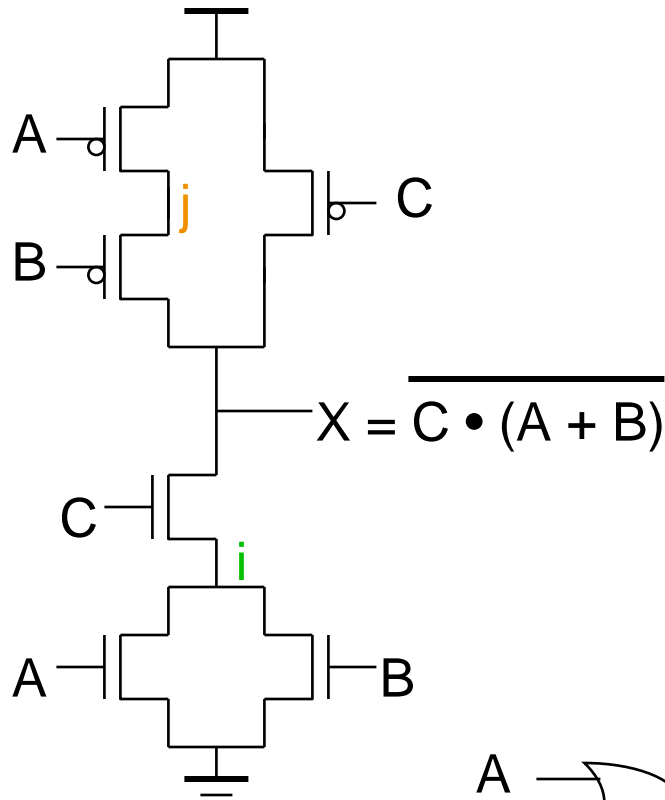
Inverter



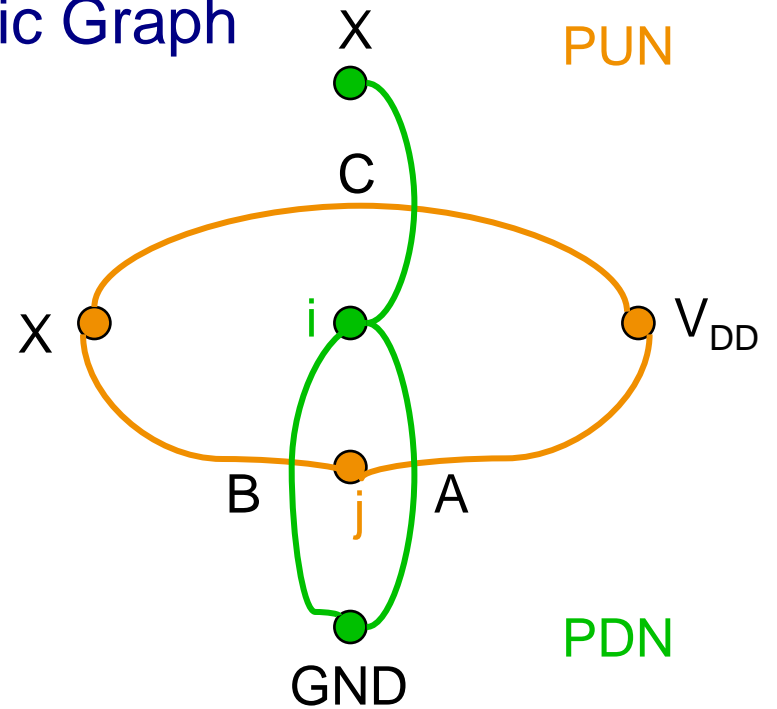
NAND2



Logic Graphs



Logic Graph





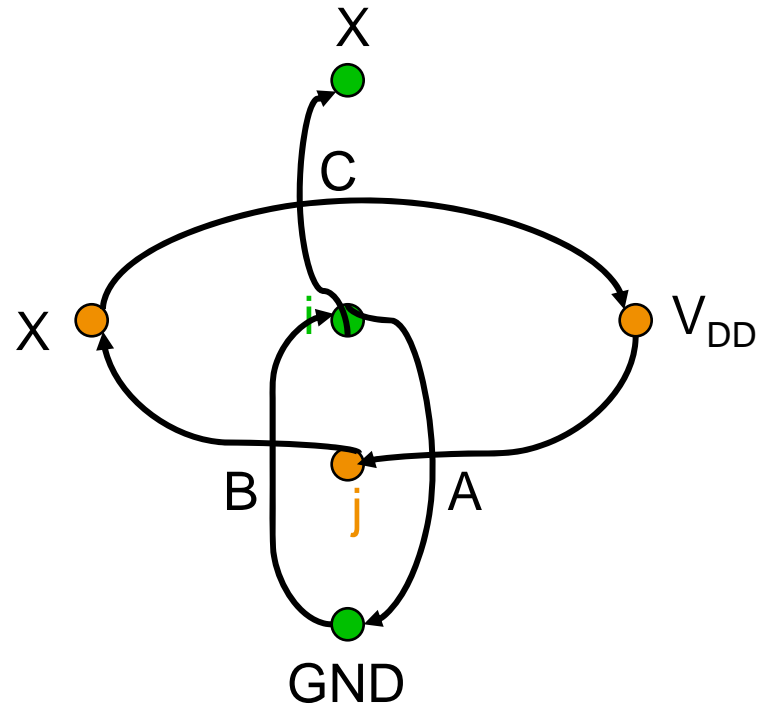
Consistent Euler Path

A B C

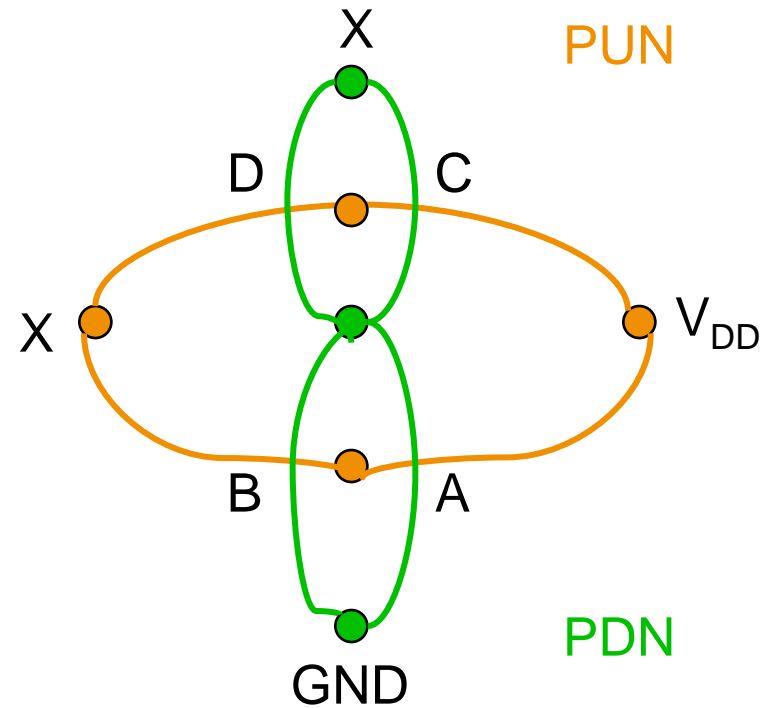
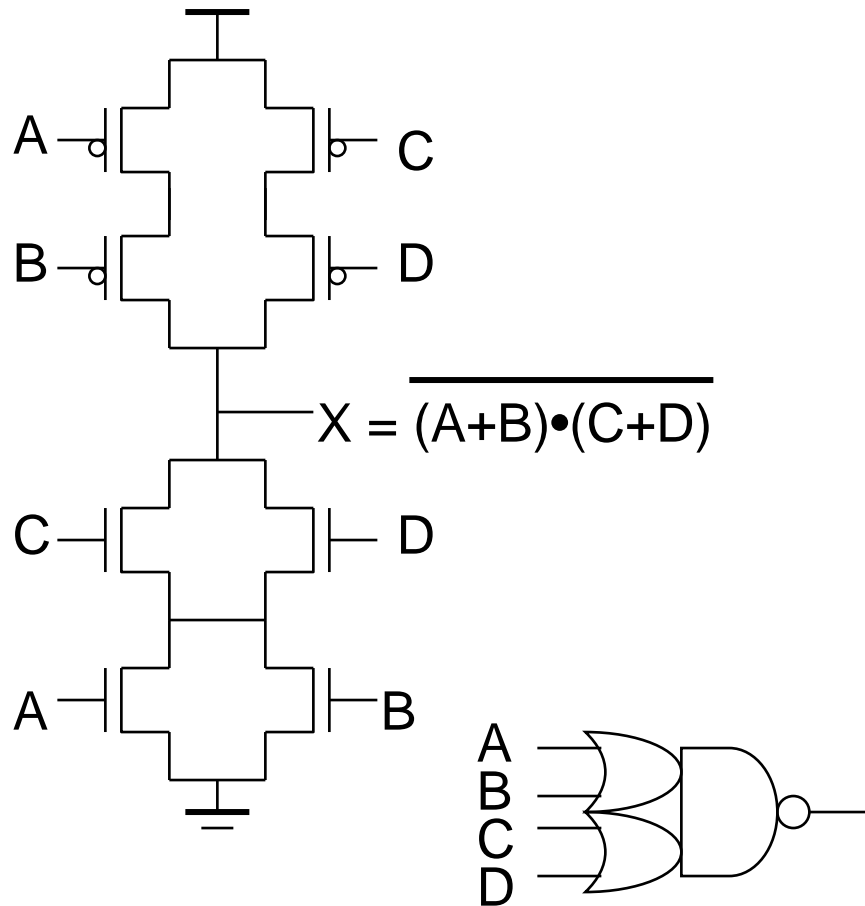
Has PDN and PUN

B C A

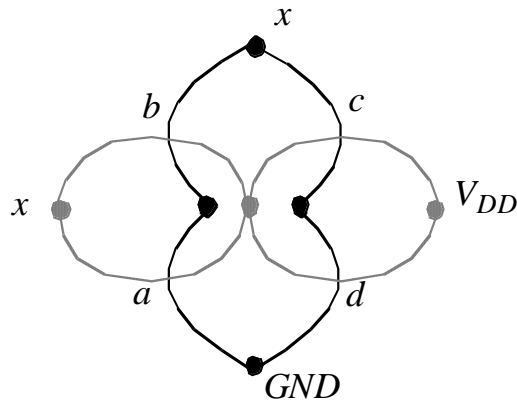
Has PUN, but no PDN



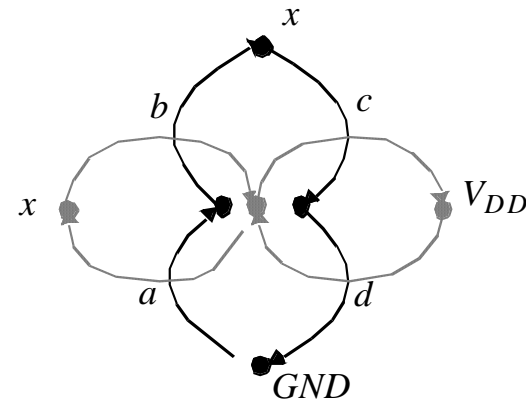
OAI22 Logic Graph



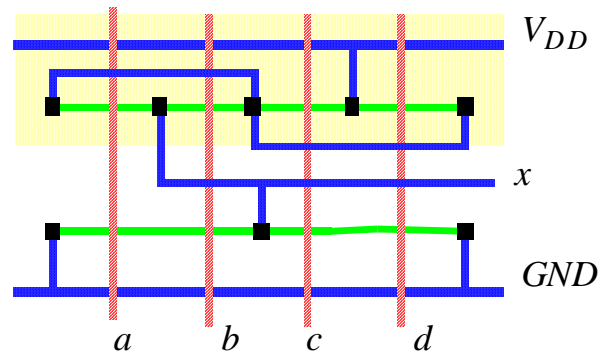
Example: $x = ab + cd$



(a) Logic graphs for $\overline{ab+cd}$



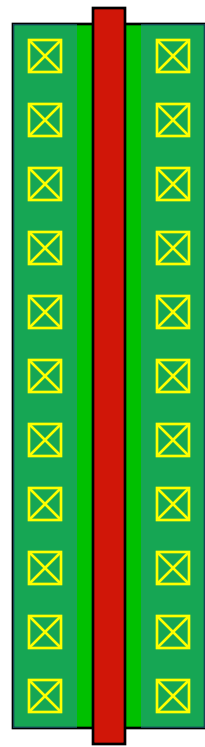
(b) Euler Paths $\{a b c d\}$



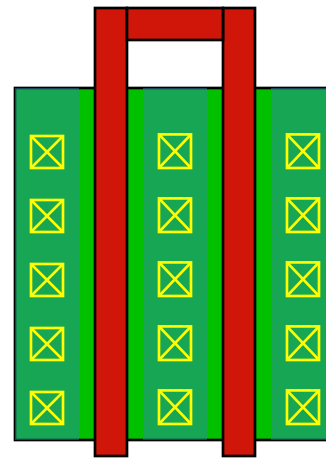
(c) stick diagram for ordering $\{a b c d\}$

Multi-Fingered Transistors

One finger



Two fingers (folded)



Less diffusion capacitance

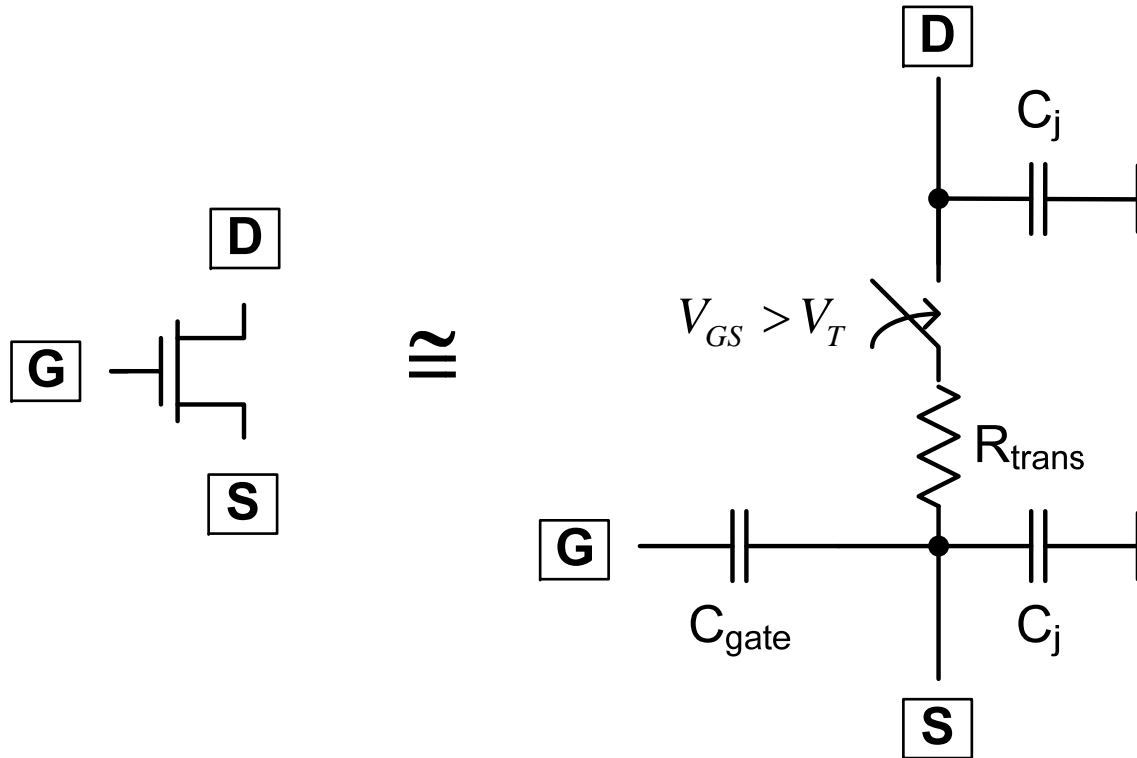
CMOS Properties

- ❑ Full rail-to-rail swing; **high noise margins**
- ❑ Logic levels not dependent upon the relative device sizes; **ratioless**
- ❑ Always a path to Vdd or Gnd in steady state; **low output impedance**
- ❑ Extremely **high input resistance**; nearly zero steady-state input current
- ❑ No direct path steady state between power and ground; **no static power dissipation**
- ❑ Propagation delay function of load capacitance and resistance of transistors

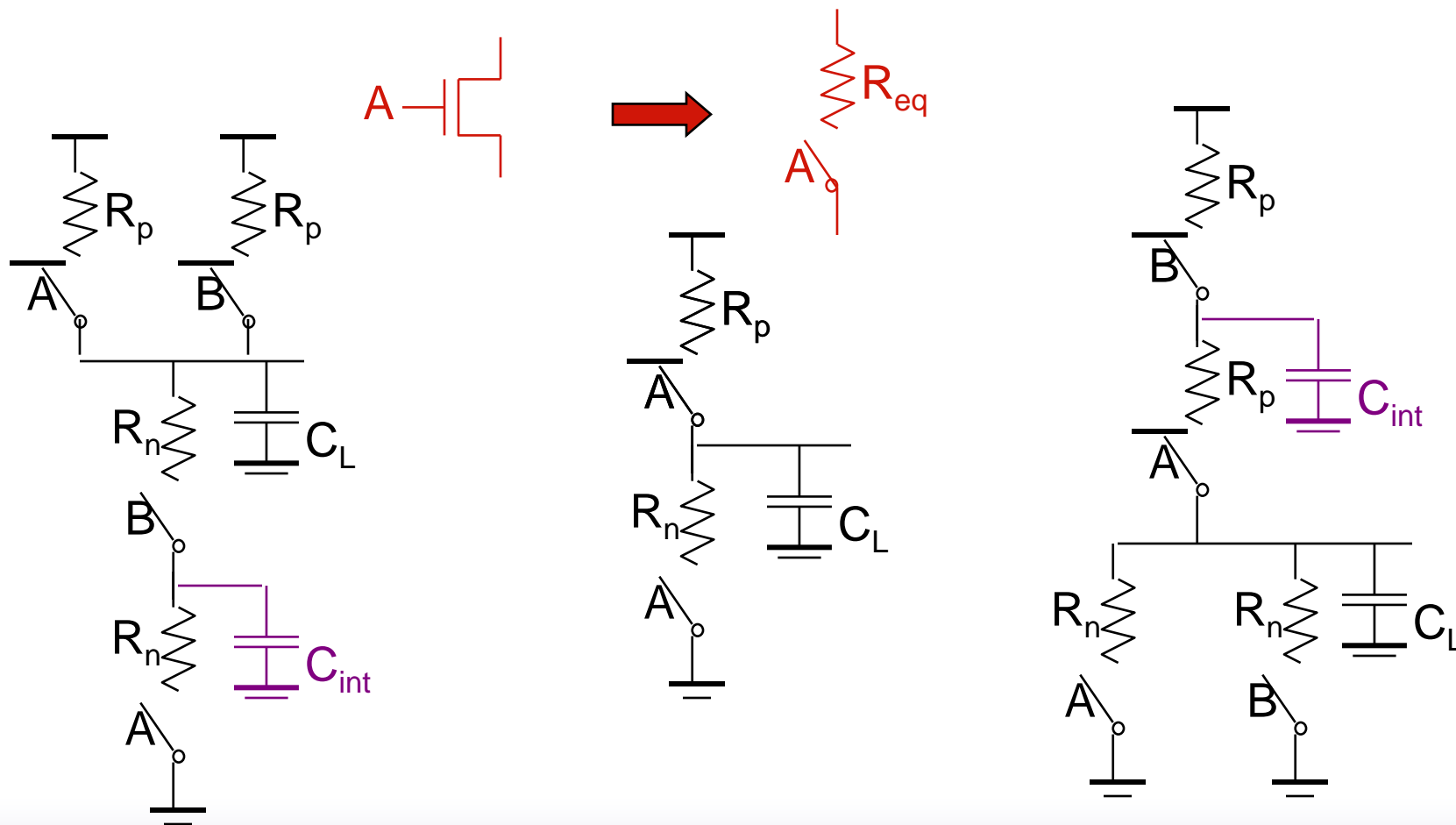


Static CMOS Design

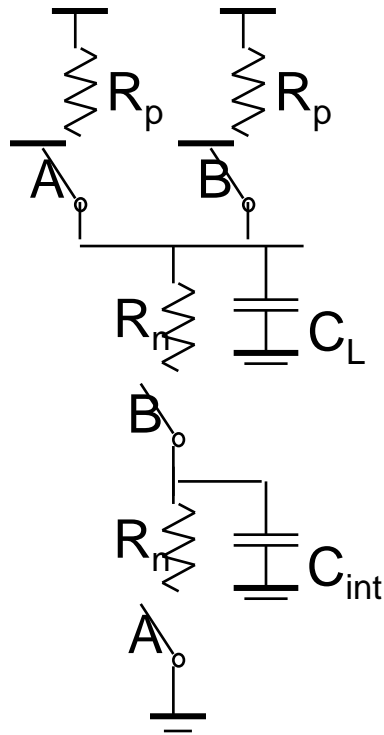
Review: Transistor Switch Model



Switch Delay Model



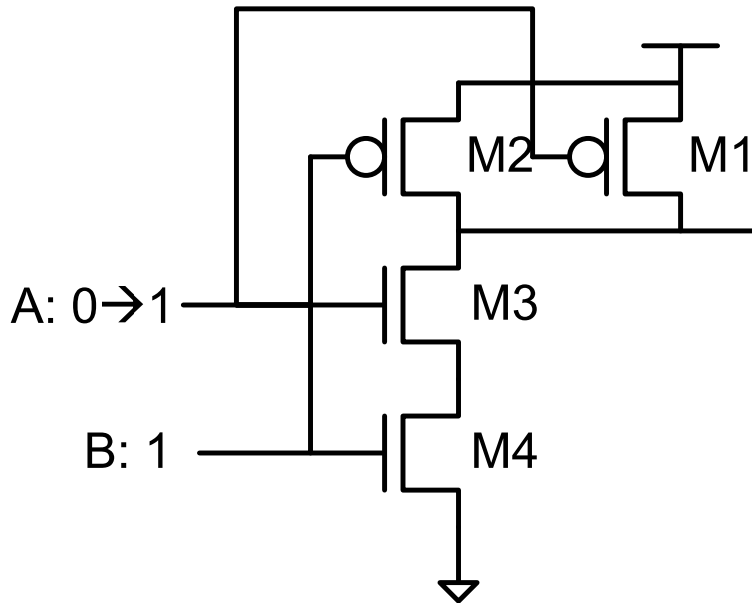
Input Pattern Effects on Delay



- Delay is dependent on the **pattern** of inputs
 - Both R and C vary with input pattern
- Low to high transition
 - both inputs go low
 - Resistance is $R_p/2$
 - one input goes low
 - Resistance is R_p
- High to low transition
 - both inputs go high
 - Resistance is $2R_n$

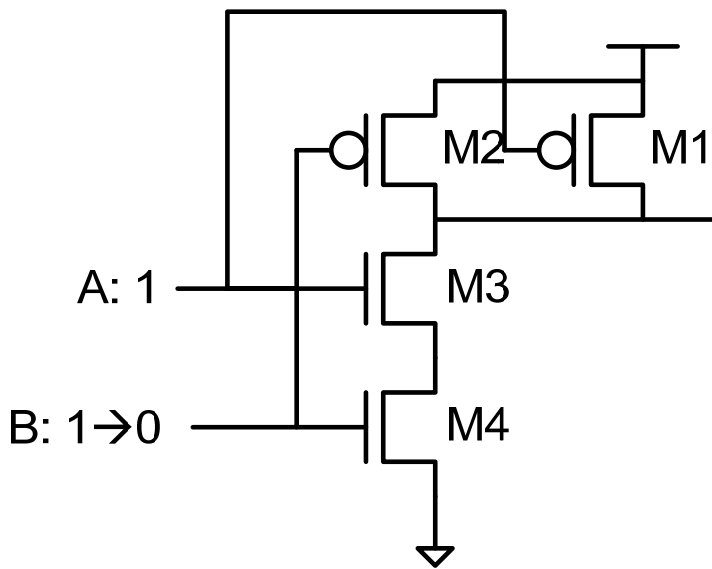
Delay Dependence on Input Pattern

- Use RC model to estimate delay



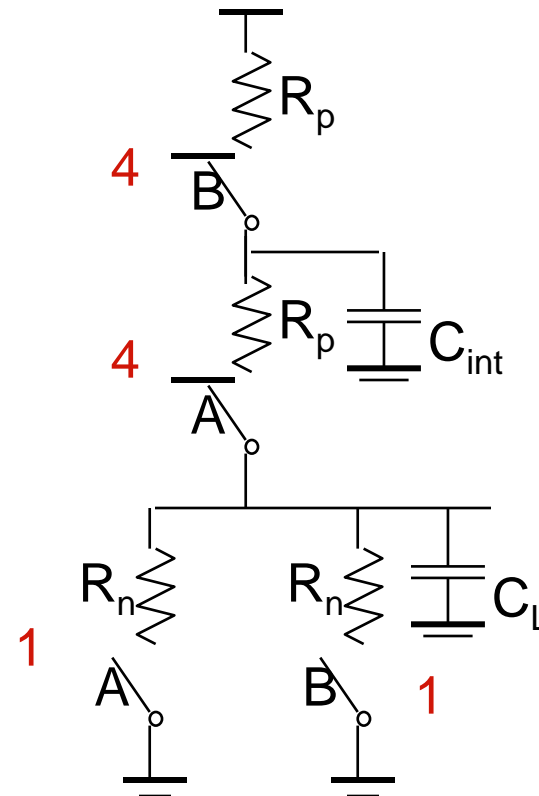
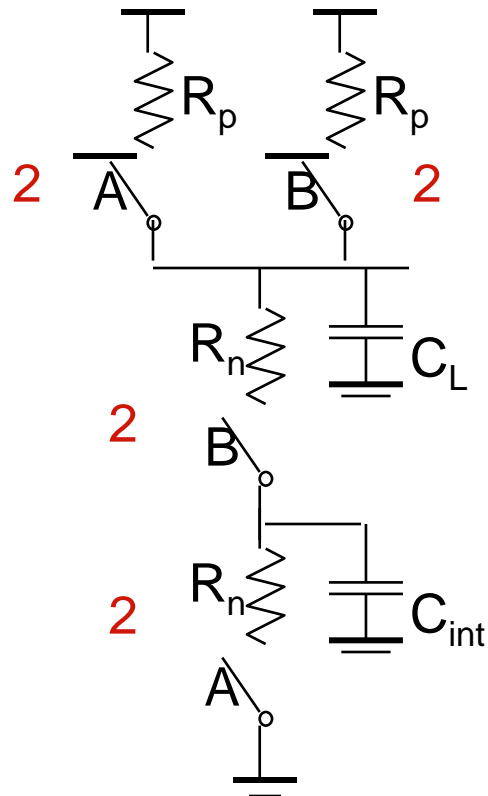
Delay Dependence on Input Pattern

- Use RC model to estimate delay



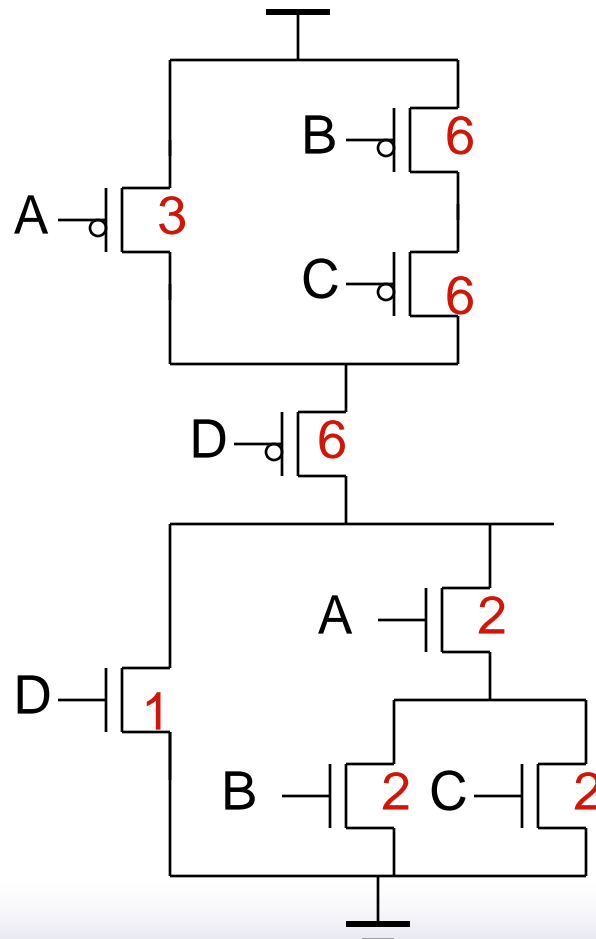


Transistor Sizing





Transistor Sizing a Complex CMOS Gate



$$\text{OUT} = \overline{D + A \cdot (B + C)}$$

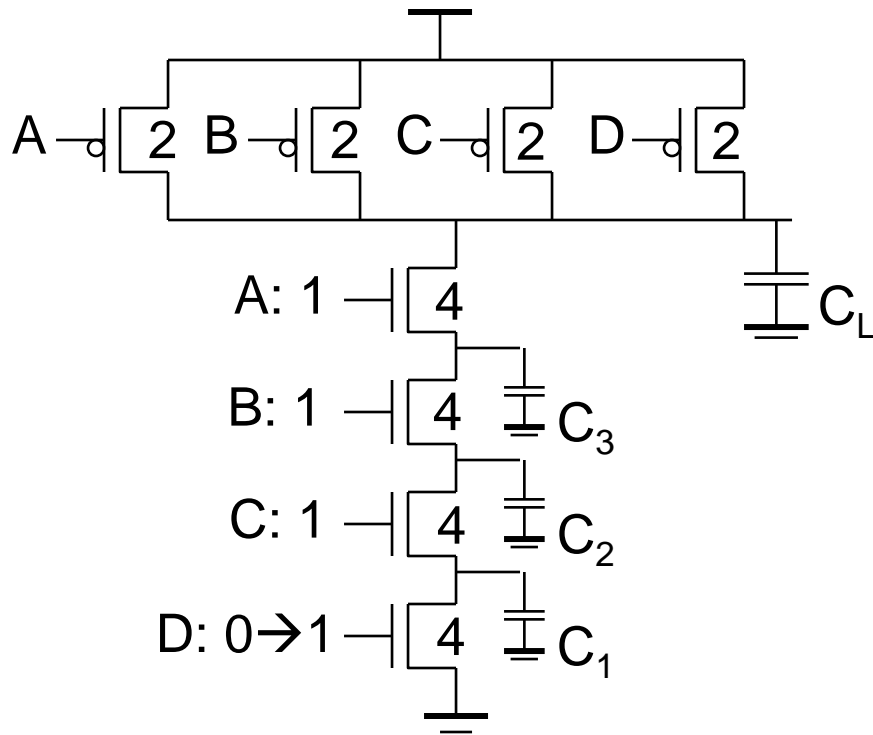
Note on Transistor Sizing

- So far, we have assumed that MOSFETs behave like linear resistor when we put two of them in series
 - I.e., I_{DSAT} of stack of 2 transistors = $\frac{1}{2} I_{\text{DSAT}}$ of single transistor
- With velocity saturated devices, this is not the case
 - More in future homeworks

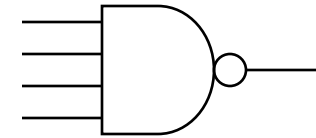
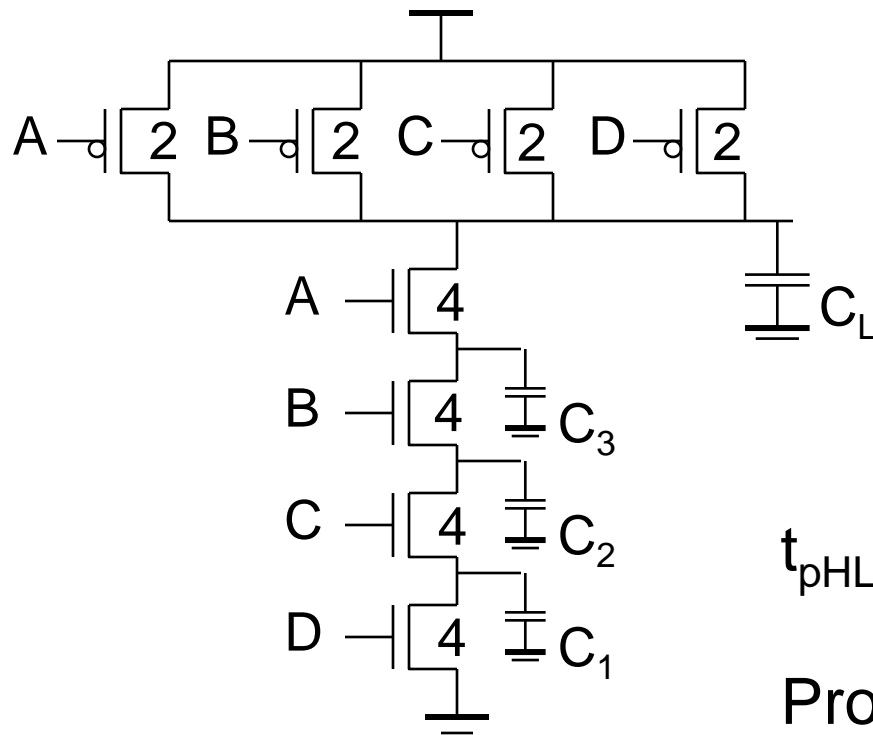


Fan-In Considerations

RC model:



Fan-In Considerations

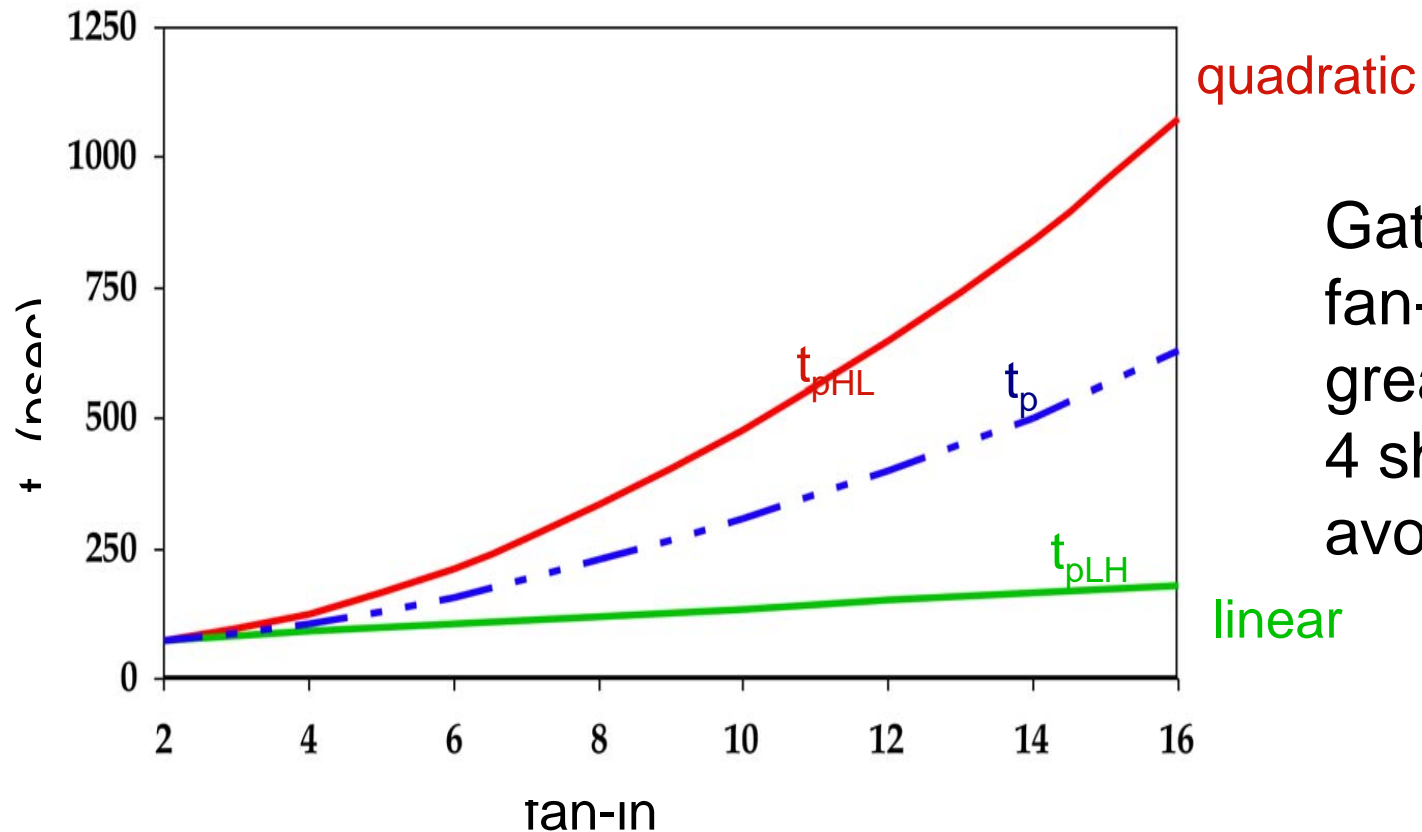


Distributed RC model
(Elmore delay)

$$t_{pHL} = 0.69 R_{eqn}(C_1 + 2C_2 + 3C_3 + 4C_L)$$

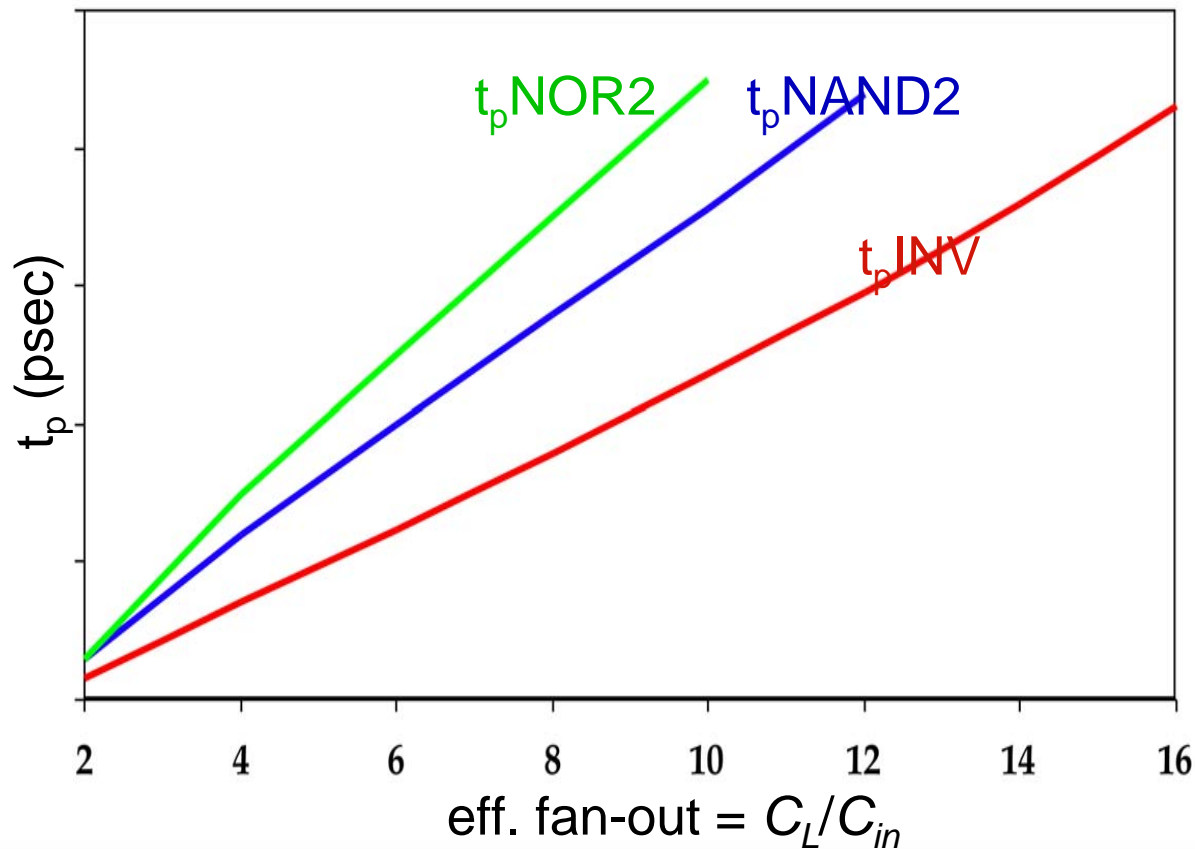
Propagation delay deteriorates rapidly as a function of fan-in – **quadratically** in the worst case.

t_p as a Function of Fan-In



Gates with a fan-in greater than 4 should be avoided.

t_p as a Function of Fan-Out



All gates have the same drive current.

Slope is a function of “driving strength”



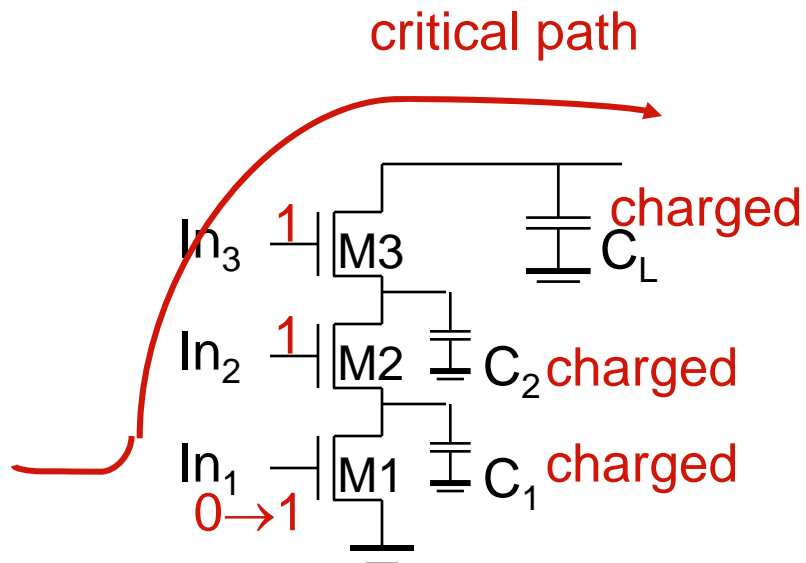
t_p as a Function of Fan-In and Fan-Out

- Fan-in: **quadratic** due to increasing resistance and capacitance
- Fan-out: each additional fan-out gate adds **two** gate capacitances to C_L

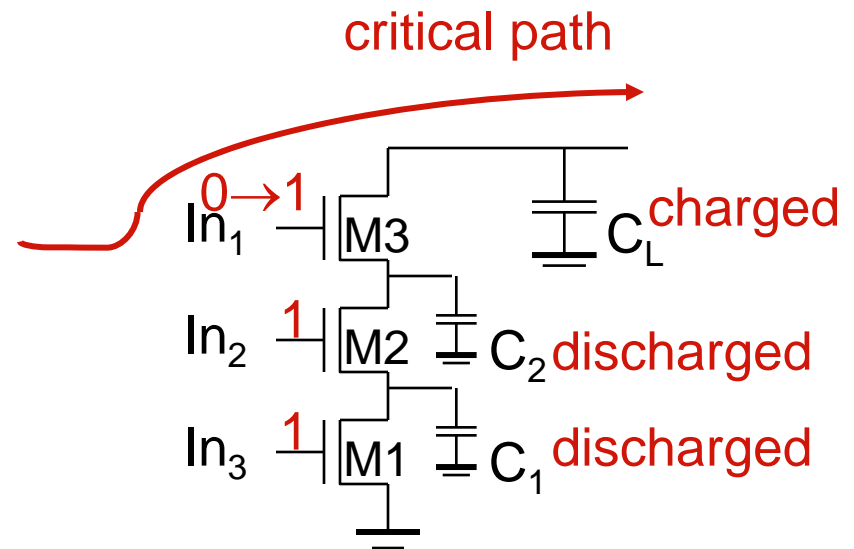
$$t_p = a_1 FI + a_2 FI^2 + a_3 FO$$

Fast Complex Gates: Design Technique 2

□ Transistor ordering



delay determined by time to discharge C_L , C_1 and C_2



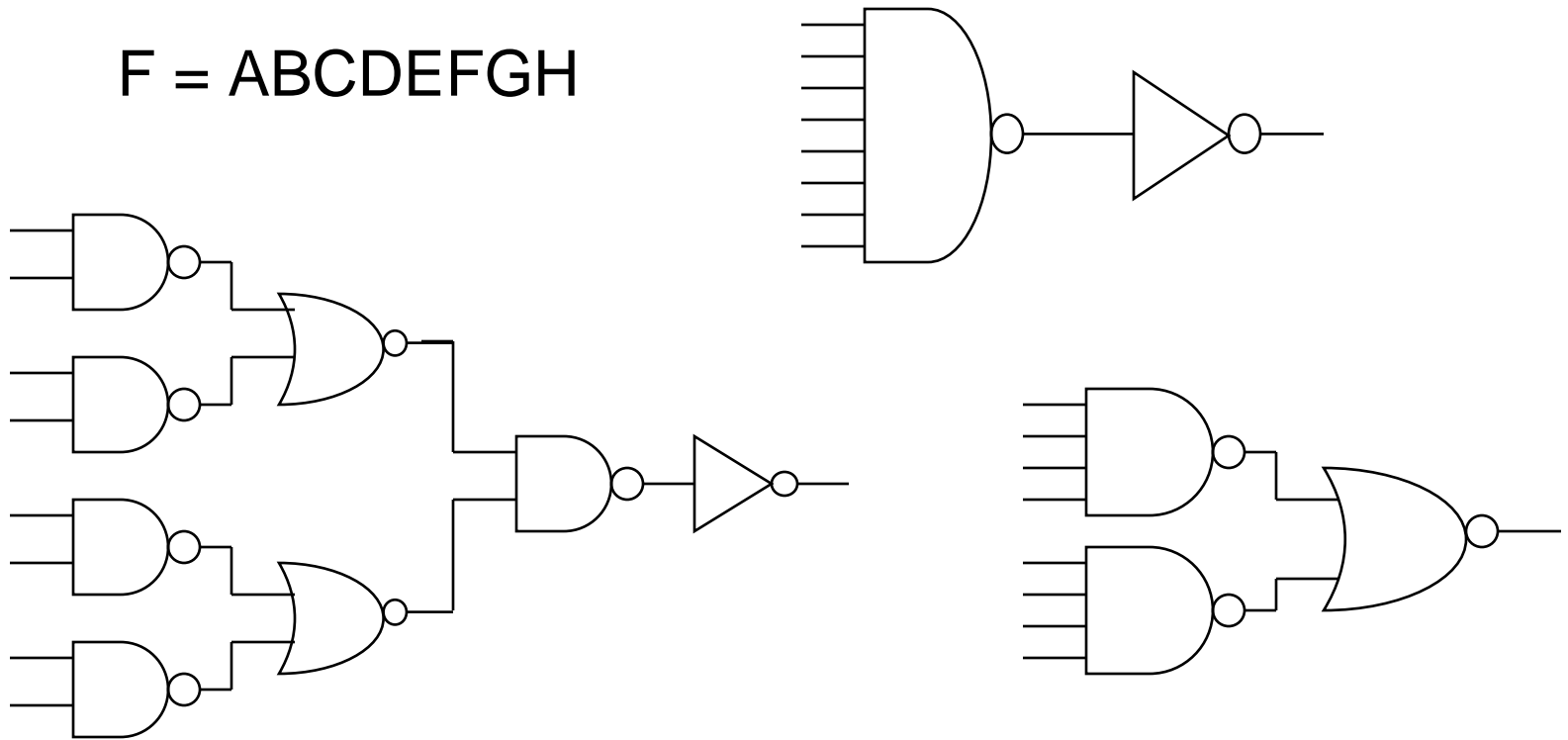
delay determined by time to discharge C_L



Fast Complex Gates: Design Technique 3

□ Alternate logic structures

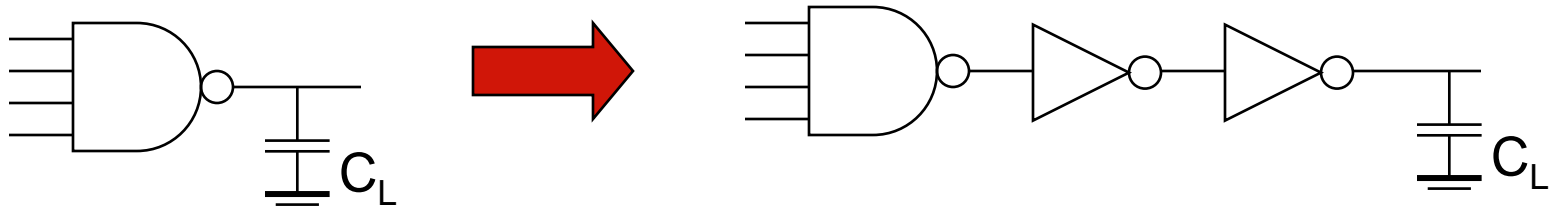
$$F = ABCDEFGH$$





Fast Complex Gates: Design Technique 4

- Isolating fan-in from fan-out using buffer insertion



Fast Complex Gates: Design Technique 5

- Reducing the voltage swing

$$t_{pHL} = 0.5 (C_L V_{DD}) / I_{DSATn}$$

$$= 0.5 (C_L V_{swing}) / I_{DSATn}$$

- linear reduction in delay
 - also reduces power consumption
- But the following gate is slower!
 - Or requires use of “sense amplifiers” on the receiving end to restore the signal level (memory design)