EE141-Spring 2008 Digital Integrated Circuits

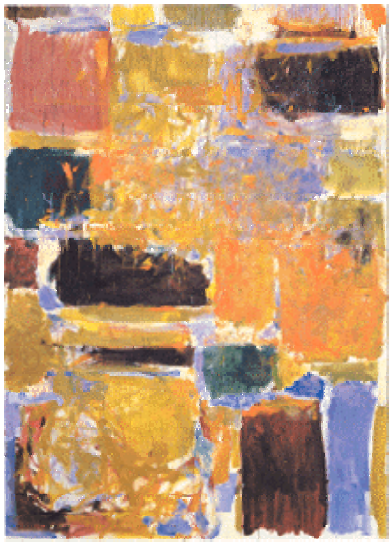
Lecture 27: Memory

Announcements

- Congratulations on the project! Superb effort.
- Final Friday May 16 5-8pm, 106 Stanley Hall
- Review Session We May 14 6-7:30pm, 203 McLaughlin

Material

- Last Lecture: Clock and Power Distribution
- This Lecture: Memory and Future Perspectives



Semiconductor Memory

Semiconductor Memory Classification

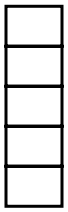
Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM	Mask-Programmed
SRAM	FIFO	E^2PROM	Programmable (PROM)
DRAM	LIFO	FLASH	
	Shift Register		
	CAM		

Random Access Memories (RAM)

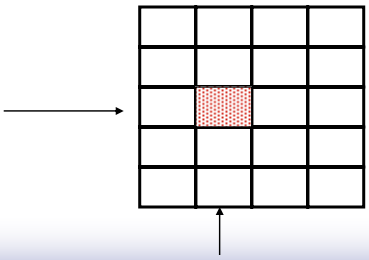
- **STATIC (SRAM)**
  - **Data stored as long as supply is applied**
  - **Larger (6 transistors/cell)**
  - **Fast**
  - **Differential (usually)**
- **DYNAMIC (DRAM)**
  - **Periodic refresh required**
  - **Smaller (1-3 transistors/cell)**
  - **Slower**
  - **Single Ended**

Random Access Chip Architecture

- Conceptual: linear array
  - Each box holds some data
  - But this does not lead to a nice layout shape
  - Too long and skinny



- Create a 2-D array
  - Decode Row and Column address to get data



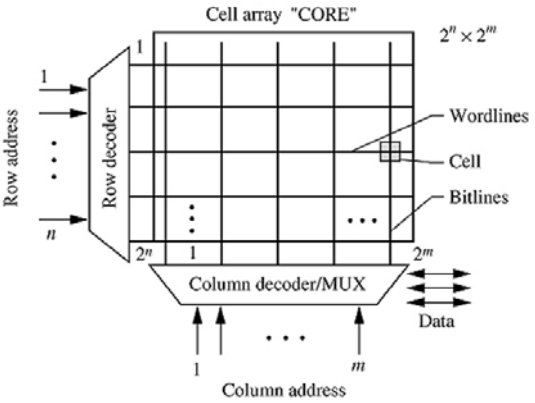
Basic Memory Array

CORE:
- keep square within a 2:1 ratio
- rows are **word lines**
- columns are **bit lines**
- data in and out on columns

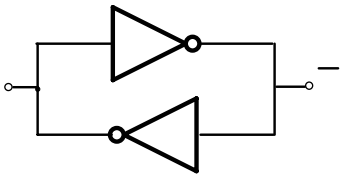
DECODERS:
- needed to reduce total number of pins; N+M address lines for 2^{N+M} bits of storage

Ex: if N+M=20 → 2^{20}= 1Mb

MULTIPLEXING:
- used to select one or more columns for input or output of data

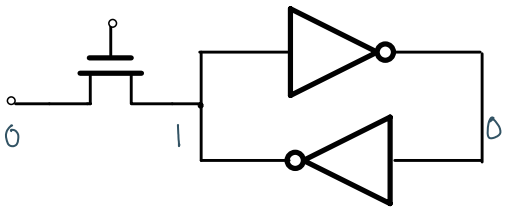


Basic Static Memory Element



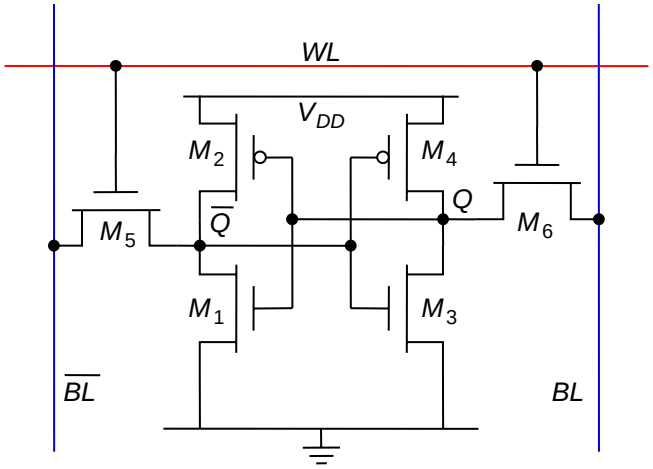
- If D is high, D_b will be driven low
  - Which makes D stay high
- Positive feedback

Writing into a Cross-Coupled Pair

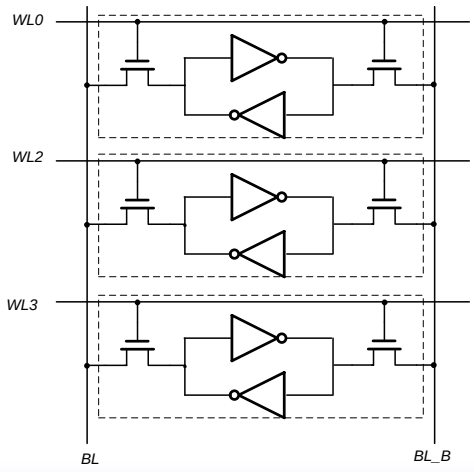


Access transistor must be able to overpower the feedback

6-transistor CMOS SRAM Cell



SRAM Column



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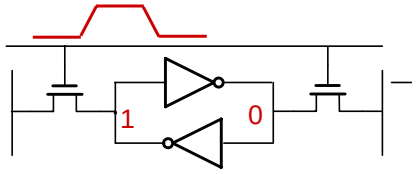
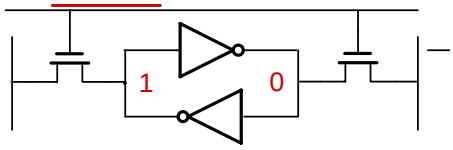
SRAM Operation

Write

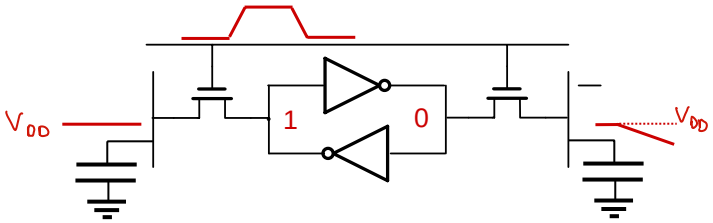


Hold



SRAM Operation

Read



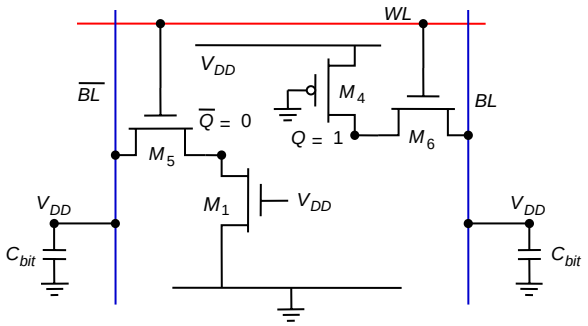
- Q_b will get pulled up when WL first goes high
  - Reading the cell should not destroy the stored value

BL

Writing a Memory Cell

Reading a Memory Cell

CMOS SRAM Analysis (Read)

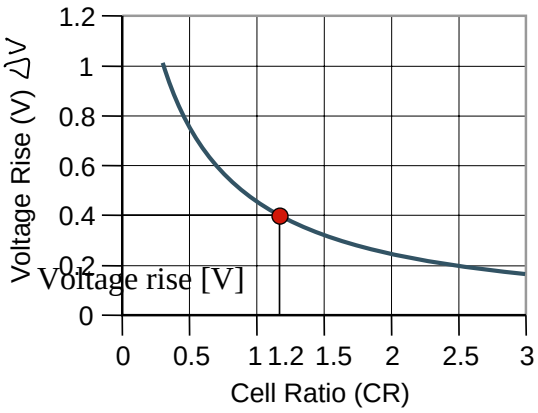


$$CR = \frac{W_1/L_1}{W_5/L_5}$$

$$k_{n,M5}\left((V_{DD} - \Delta V - V_{Tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}\right) = k_{n,M1}\left((V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}\right)$$

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{Tn}) - \sqrt{V_{DSATn}^2(1+CR) + CR^2(V_{DD} - V_{Tn})^2}}{CR}$$

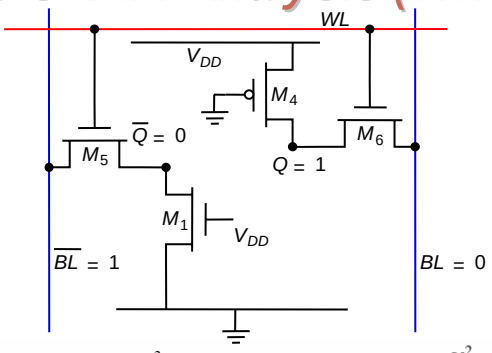
CMOS SRAM Analysis (Read)



Voltage rise [V]

$$CR = \frac{W_1/L_1}{W_5/L_5}$$

CMOS SRAM Analysis (Write)

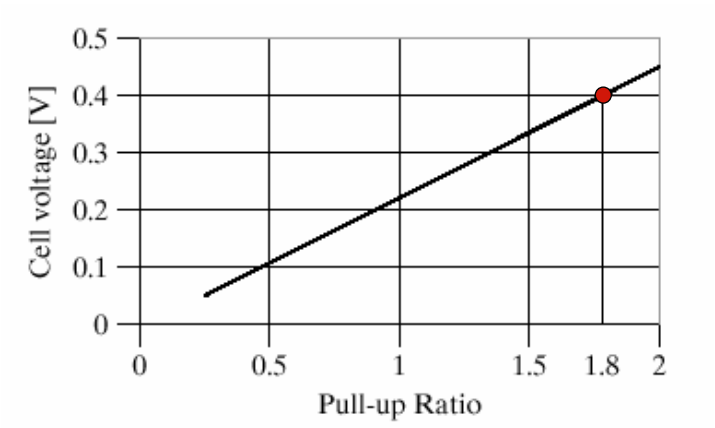


$$PR = \frac{(W/L)_4}{(W/L)_6}$$

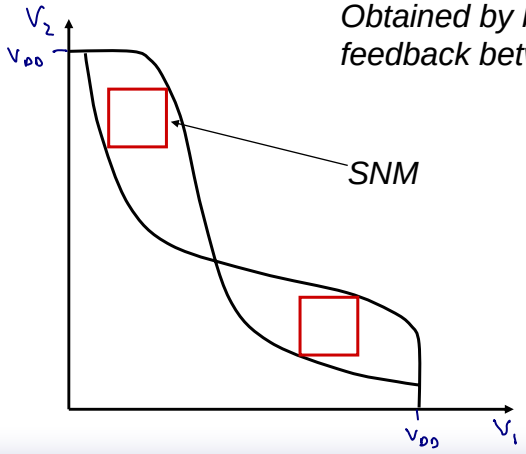
$$k_{n,M6}\left((V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2}\right) = k_{p,M4}\left((V_{DD} - |V_{Tp}|)V_{SATp} - \frac{V_{SATp}^2}{2}\right)$$

$$V_Q = V_{DD} - V_{Tn} - \sqrt{(V_{DD} - V_{Tn})^2 - 2\frac{\mu_p}{\mu_n}PR\left((V_{DD} - |V_{Tp}|)V_{SATp} - \frac{V_{SATp}^2}{2}\right)},$$

CMOS SRAM Analysis (Write)

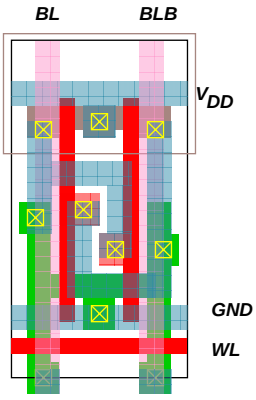


Read Static Noise Margin



Obtained by breaking the feedback between the inverters

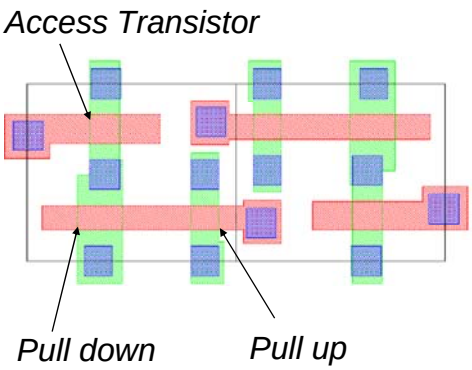
6T-SRAM — Layout

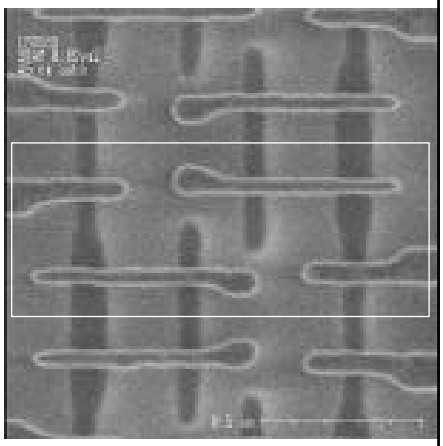


Compact cell
- Bitlines: M2
- Wordline: bootstrapped in M3

65nm SRAM

- ST/Philips/Motorola





Some other Issues in Memory Design

- Decoders
- Sense Amplifiers
- Periphery

What does the future hold?

- Scaling will go on for some time
- But will slow down …
- The good news: Design rules!