



EE141-Spring 2008

Digital Integrated Circuits

Lecture 6 Inverter VTC and Delay

Announcements

- Prof. Rabaey back next week
- Make-up lectures (will be video-taped)
 - Tu Febr 19 – 11am-12:30pm
 - Tu Febr 26 – 11am-12:30pm
- No Lab on Mo Febr 18 (President's Day).
Lab 3 starts on Tu Febr 19
- Homework #3 due We Febr 20 (due to delayed schedule)
- Homework #4 posted that same day

Class Material

- Last lecture
 - MOS transistor modeling
- Today's lecture
 - CMOS Inverter: VTC and delay
- Reading (5.1-5.3, 5.4.2)

Review: “Long-Channel” Transistor

Review: “Short-Channel” Transistor

Review: “Short-Channel” Transistor

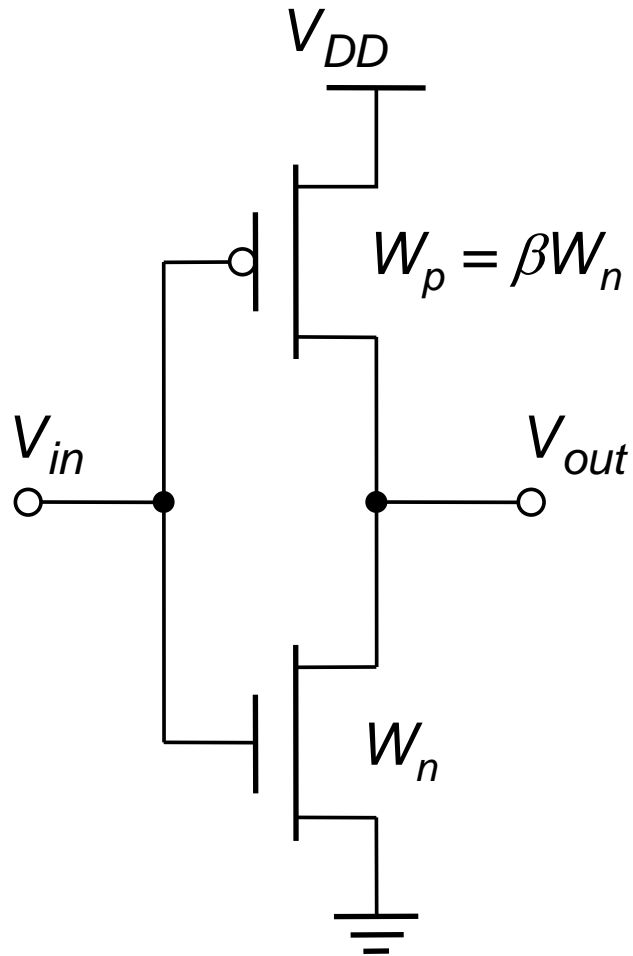
Review: “Short-Channel” Transistor

CMOS Inverter

VTC

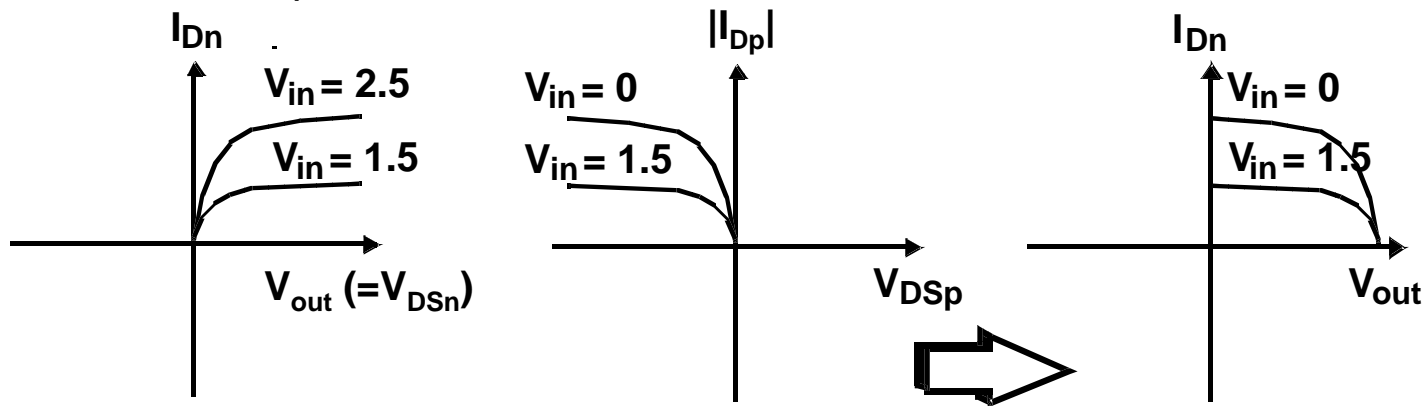


The CMOS Inverter

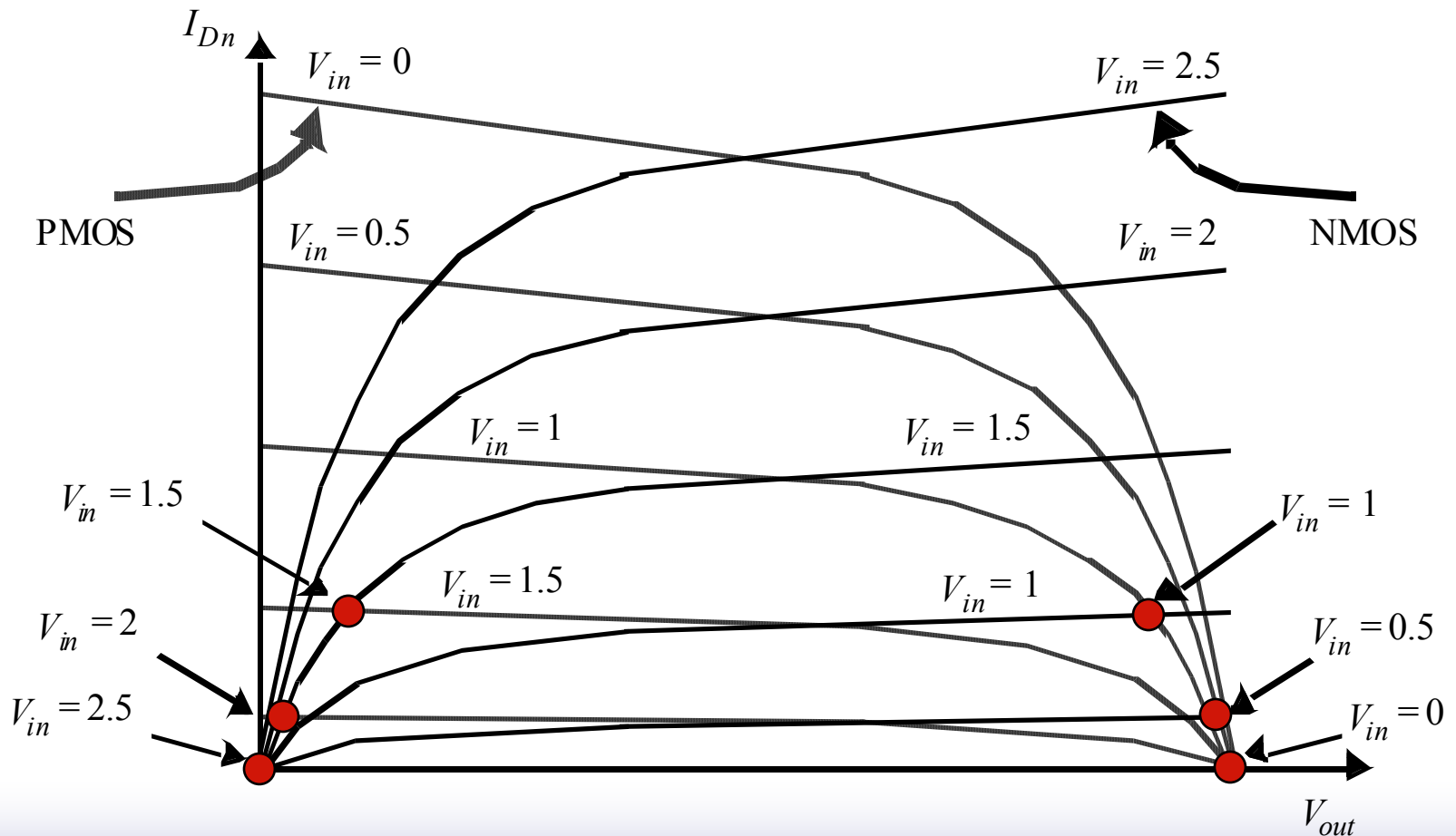


PMOS Load Lines

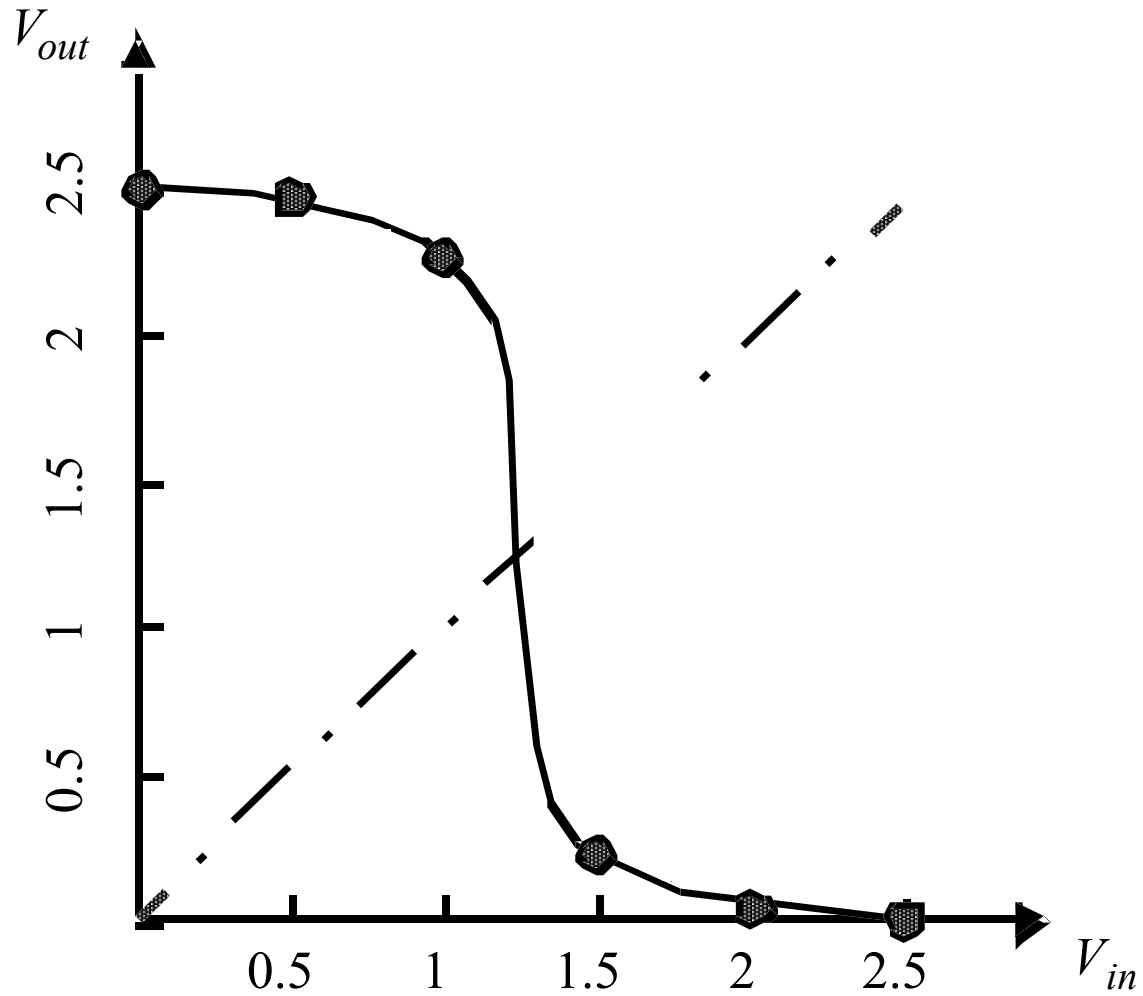
- For DC VTC, $I_{Dn} = I_{Dp}$
 - Graphically, looking for intersections of NMOS and PMOS IV characteristics
- To put IV curves on the same plot, PMOS IV is “flipped” since $|V_{DSp}| = V_{DD} - V_{out}$
 - Also, $|V_{GSpl}| = V_{dd} - V_{in}$



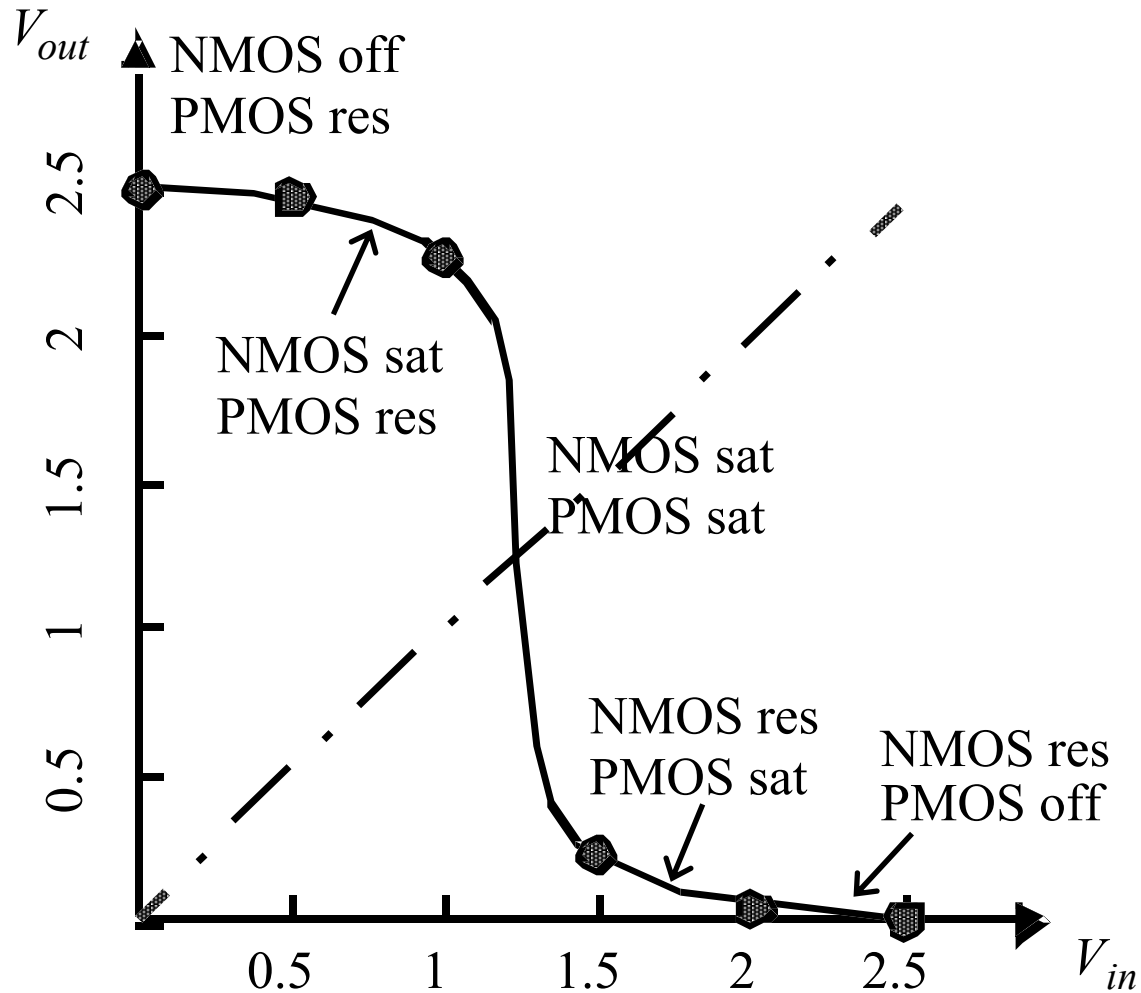
CMOS Inverter Load Characteristics



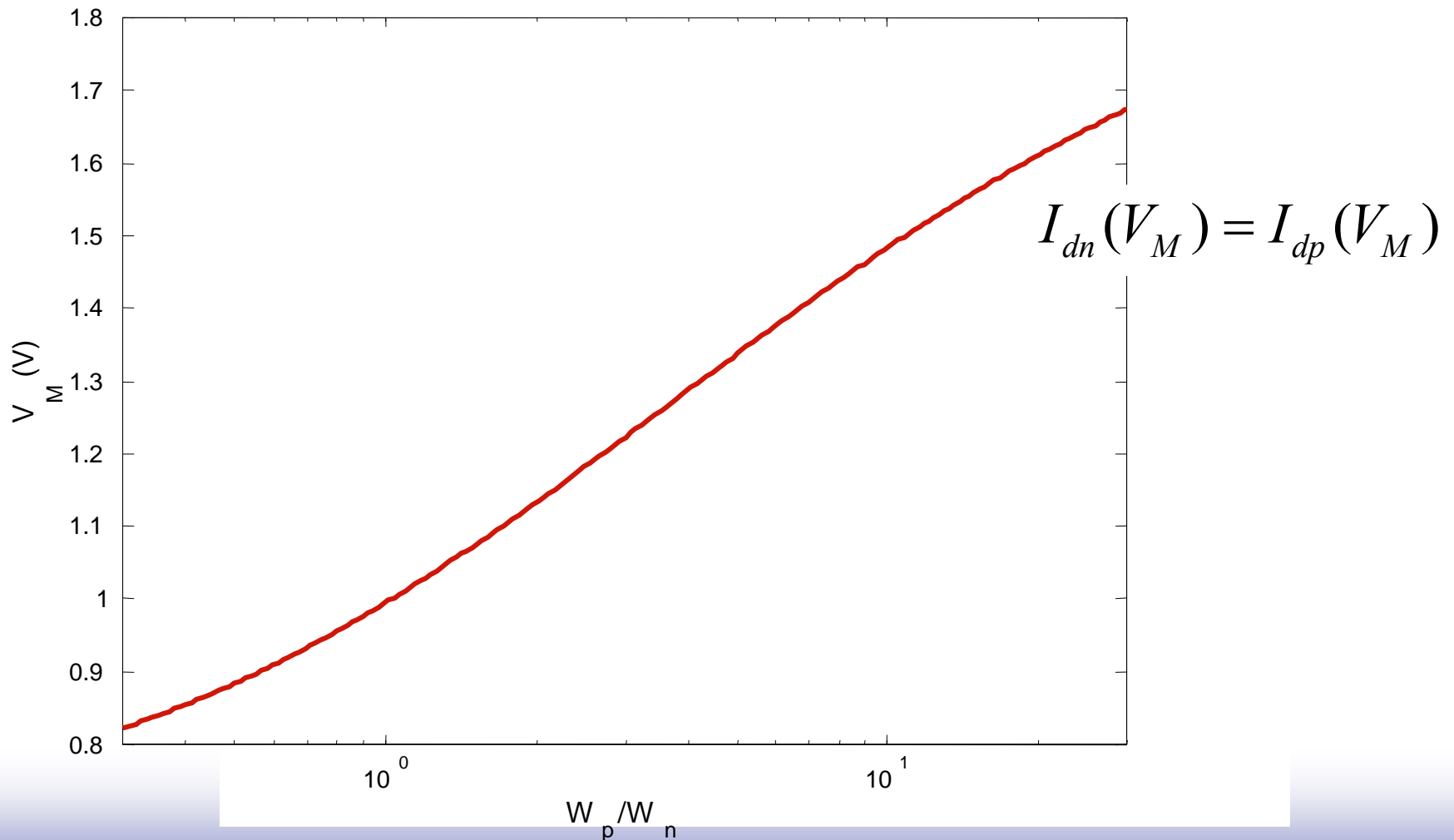
CMOS Inverter VTC



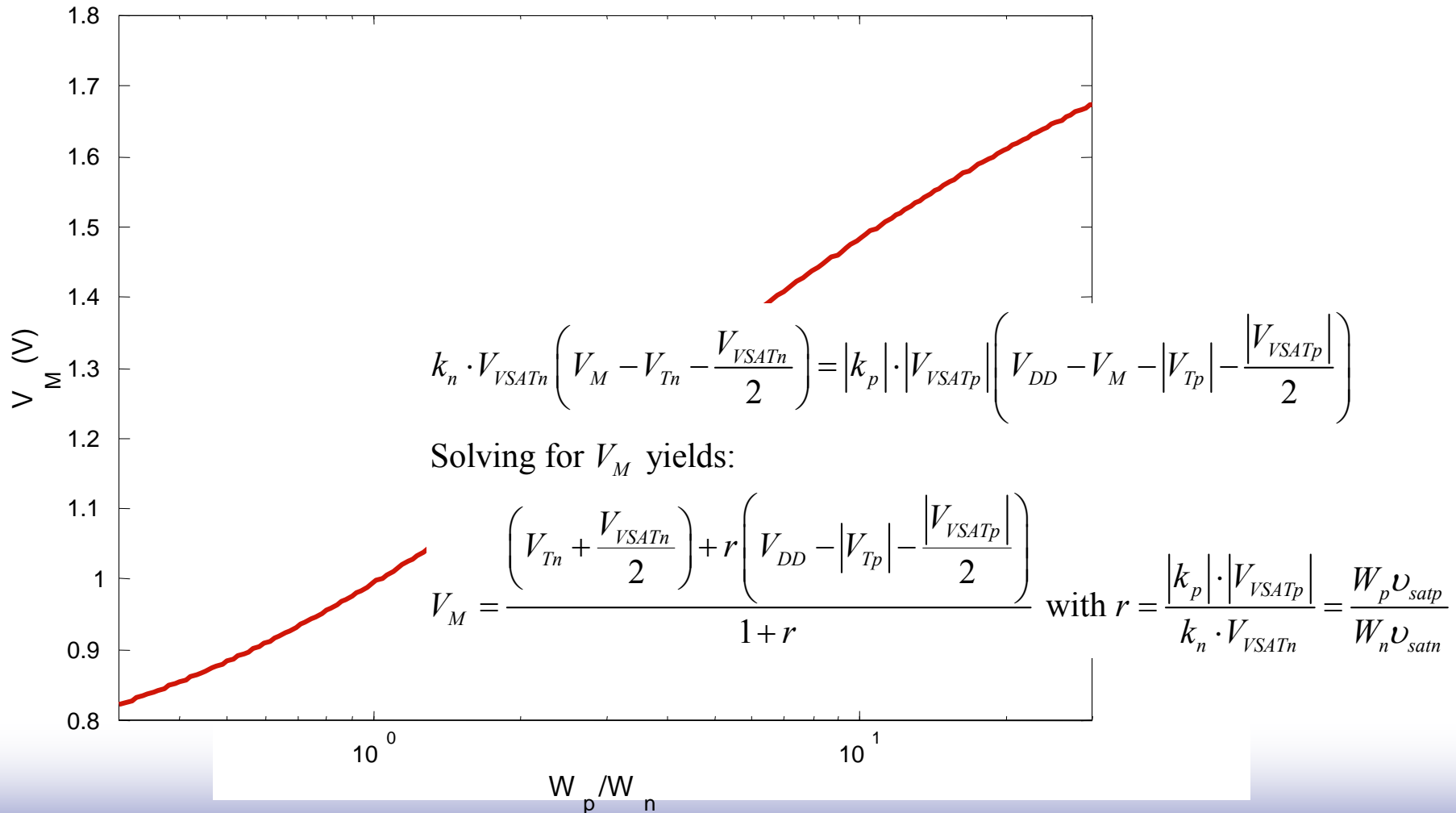
CMOS Inverter VTC



Switching Threshold as a Function of Transistor Ratio

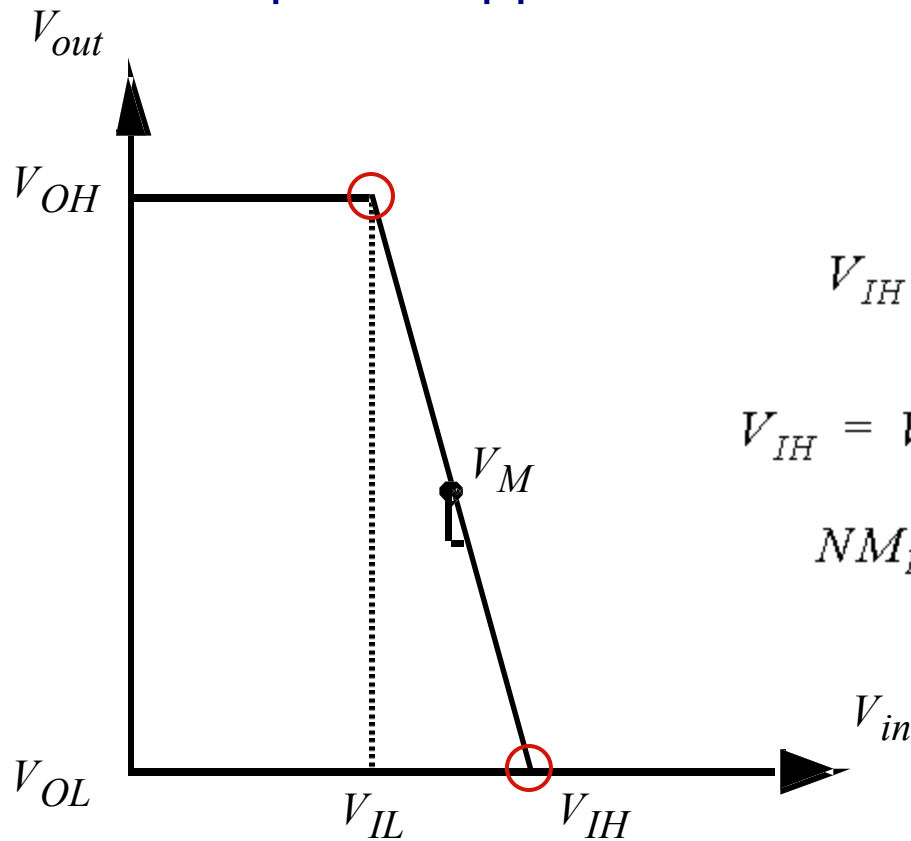


Switching Threshold as a Function of Transistor Ratio



Determining V_{IH} and V_{IL}

A simplified approach

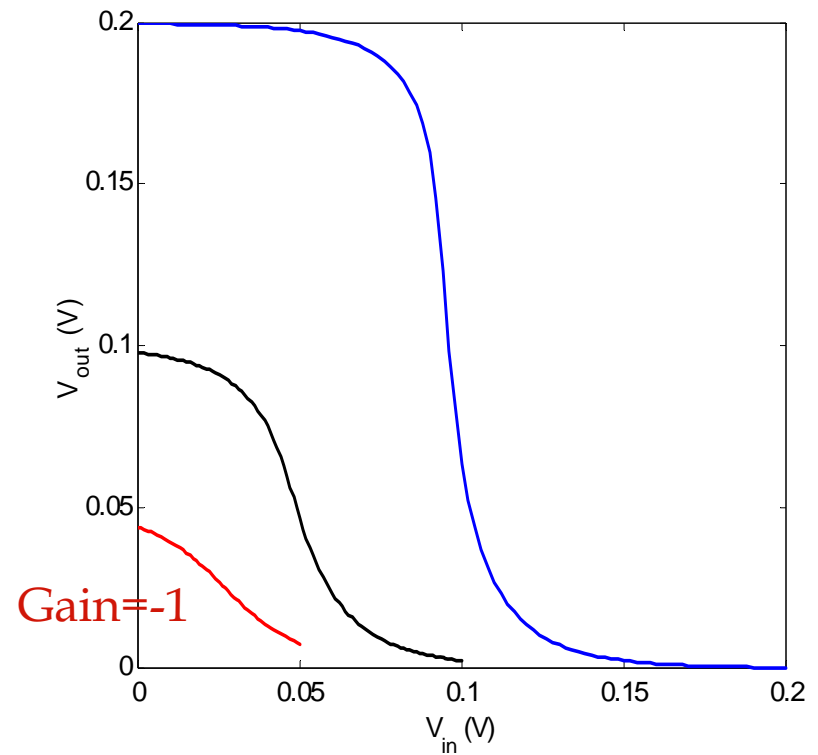
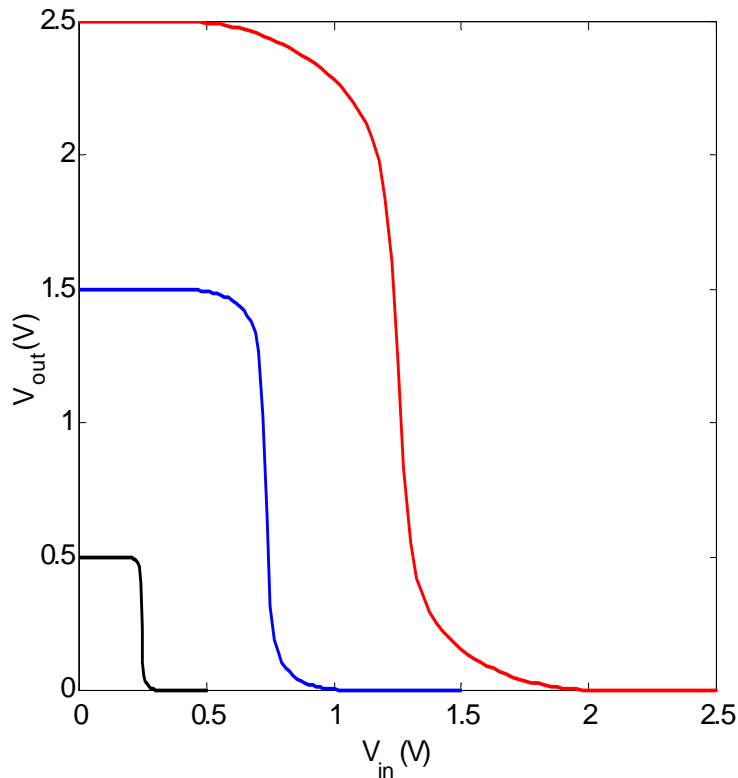


$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

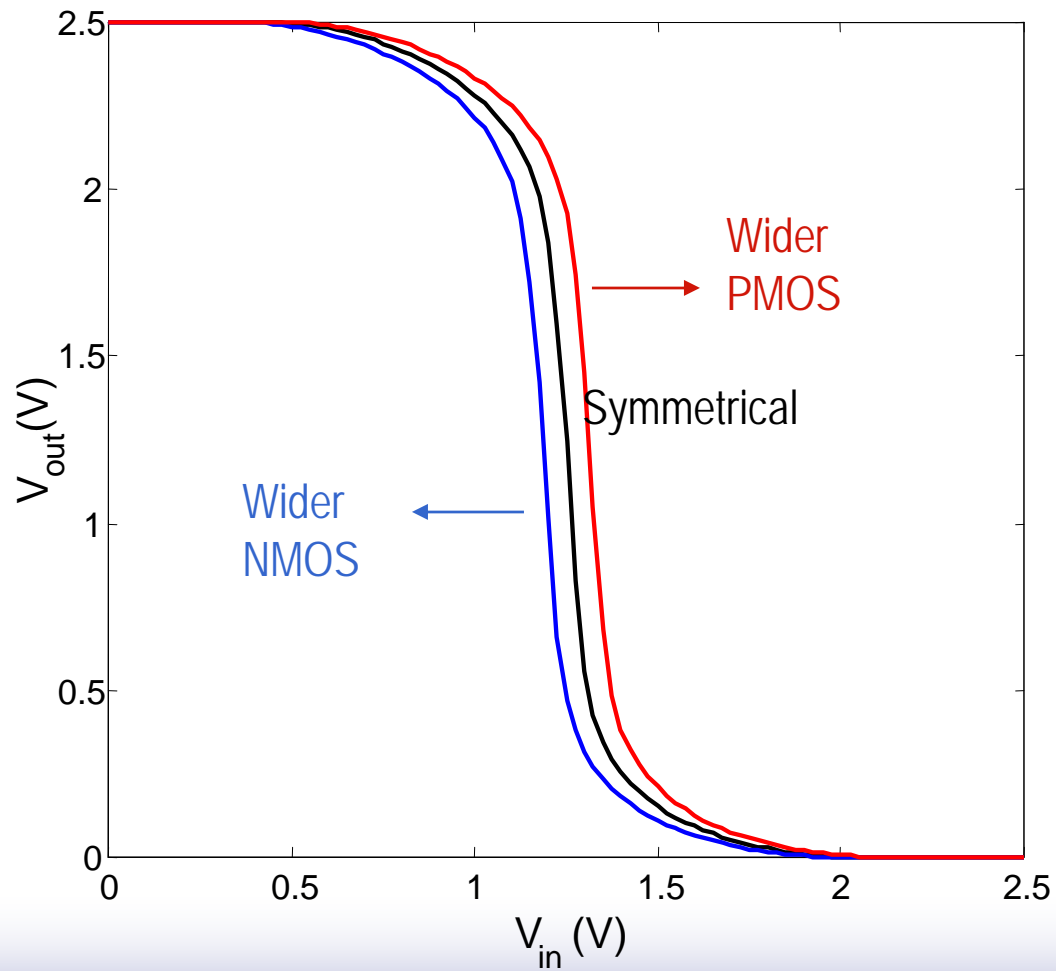
$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \quad NM_L = V_{IL}$$

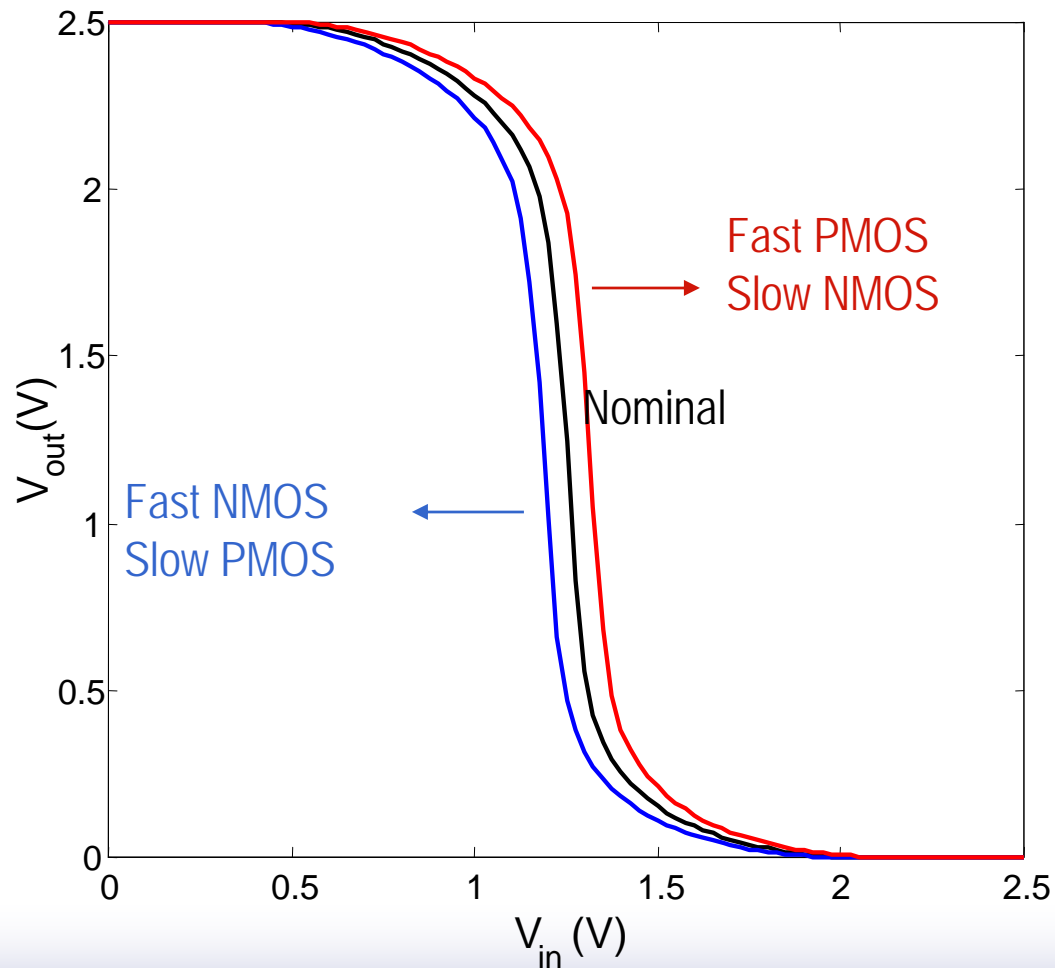
Gain as a function of VDD



Impact of Sizing



Impact of Process Variations

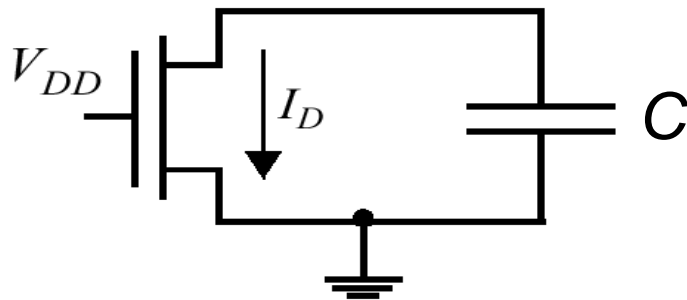


CMOS Switching



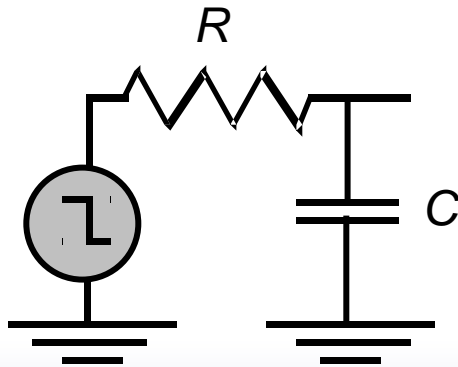
MOS Transistor as a Switch

- Discharging a capacitor



$$i_D = i_D(V_{DS})$$
$$i_D = C \frac{dV_{DS}}{dt}$$

- We modeled this with:



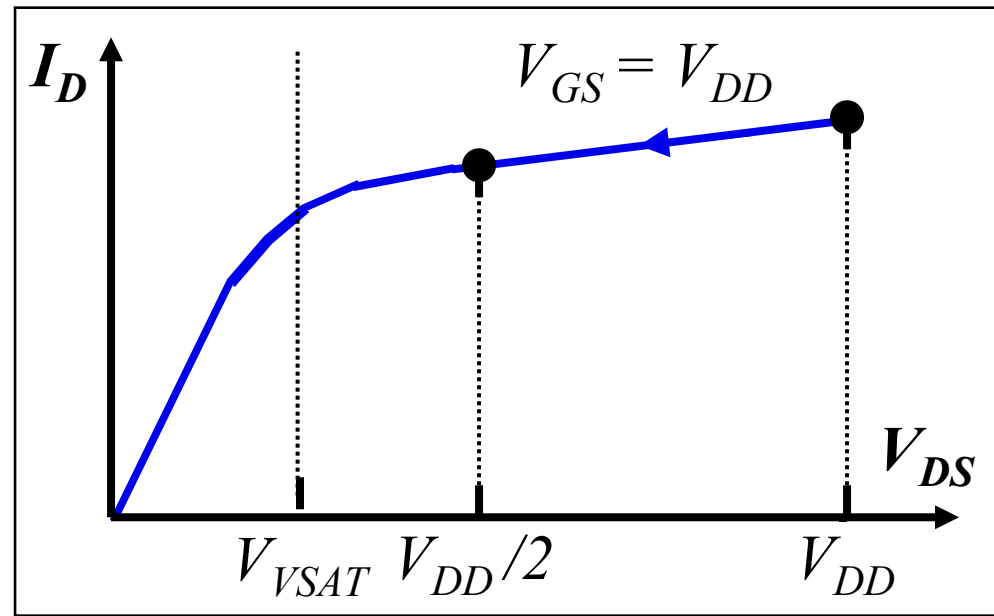
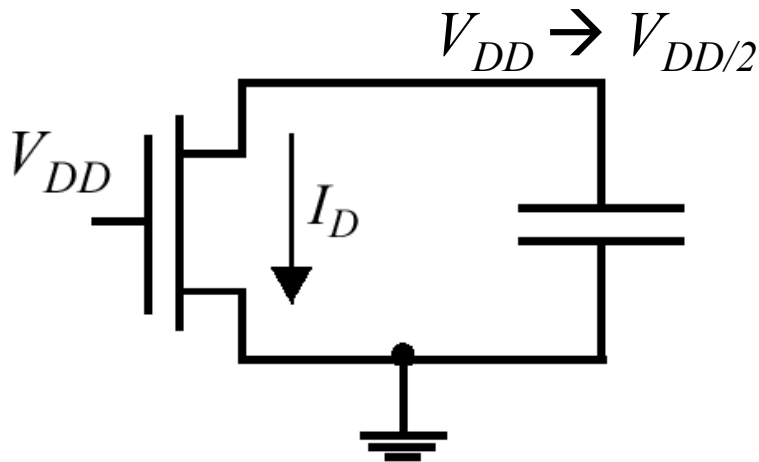
$$t_p = \ln(2) RC$$

MOS Transistor as a Switch

- Saw that real transistors aren't exactly resistors
 - Look more like current sources in saturation
- Two questions:
 - Which region of IV curve determines delay?
 - How can that match up with the RC model?

Transistor Driving a Capacitor

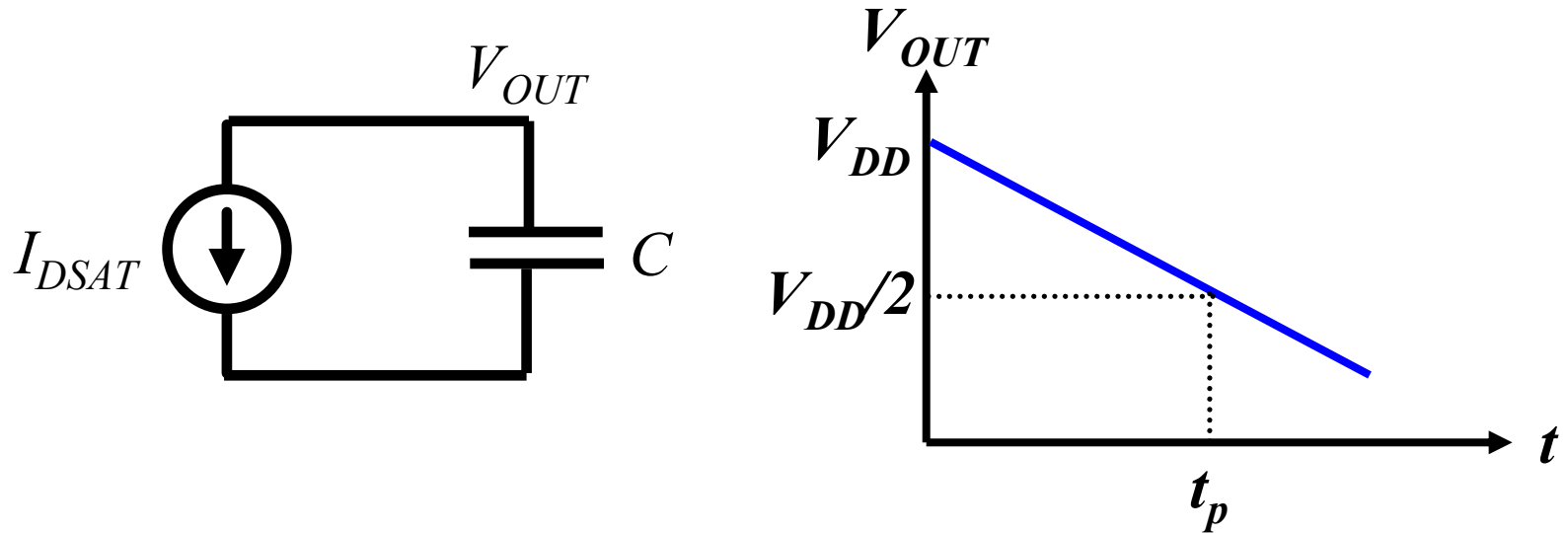
- With a step input:



- Transistor is in (velocity) saturation during entire transition from V_{DD} to $V_{DD}/2$

Switching Delay

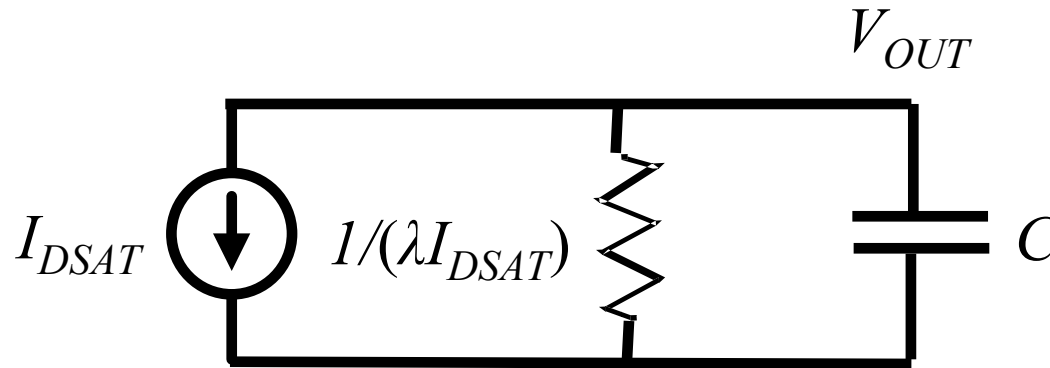
- In saturation, transistor basically acts like a current source:



$$V_{OUT} = V_{DD} - (I_{DSAT}/C)t \longrightarrow \boxed{t_p = C(V_{DD}/2)/I_{DSAT}}$$

Switching Delay (with Output Conductance)

- Including output conductance:



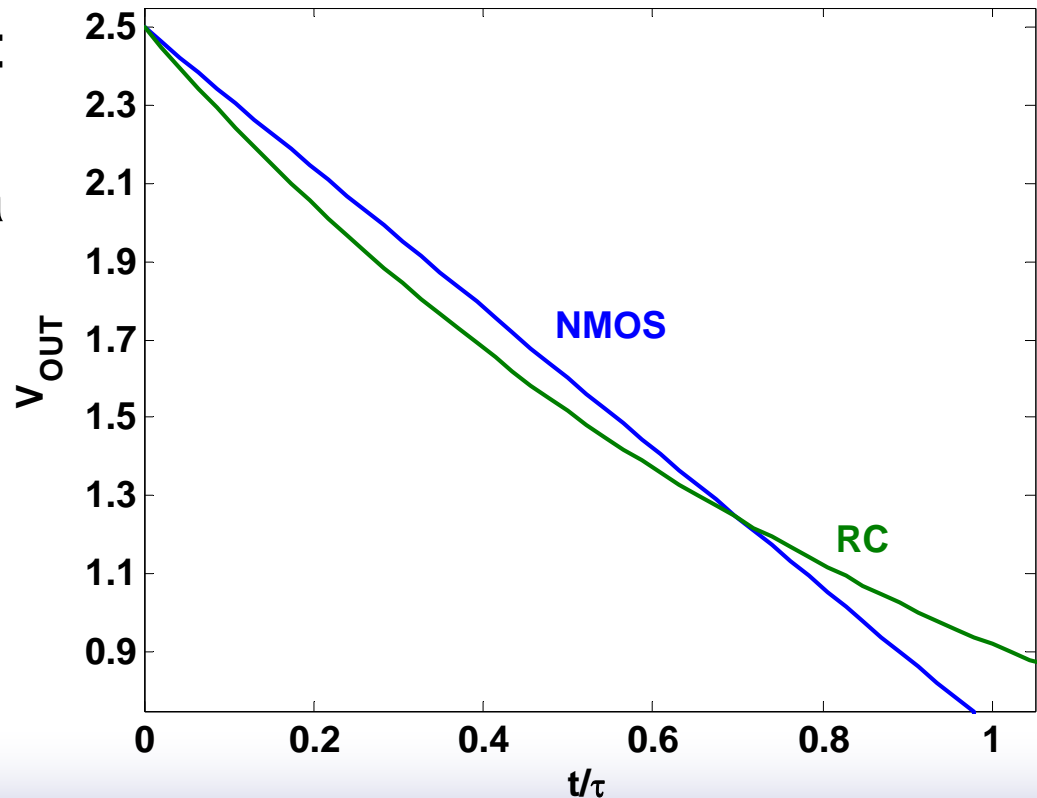
$$V_{OUT} = (V_{DD} + \lambda^{-1}) e^{-t/(C/\lambda I_{DSAT})} - \lambda^{-1}$$

- For “small” λ :

$$t_p \approx \frac{C(V_{DD}/2)}{(1 + \lambda V_{DD}) I_{DSAT}}$$

RC Model

- Transistor current not linear on V_{OUT} – how is the RC model going to work?
- Look at waveforms:
- Voltage looks like a ramp for RC too



Finding Req

- Match the delay of the RC model with the actual delay:

$$t_p = t_{p,RC}$$
$$\frac{C(V_{DD}/2)}{(1 + \lambda V_{DD}) I_{DSAT}} = \ln(2) R_{eq} C \longrightarrow R_{eq} = \frac{(V_{DD}/2)}{\ln(2)(1 + \lambda V_{DD}) I_{DSAT}}$$

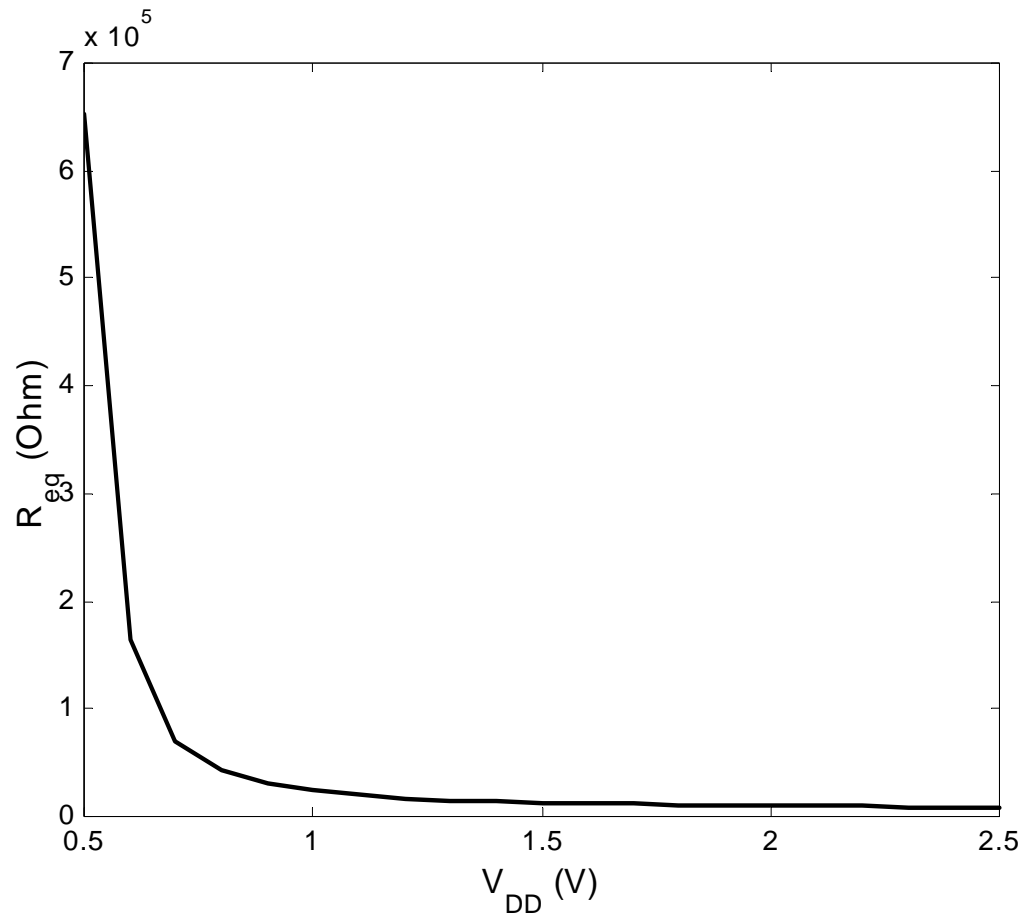
- Often just:

$$R_{eq} \approx \frac{1}{2 \cdot \ln(2)} \frac{V_{DD}}{I_{DSAT}}$$

- Note that the book uses a different method and gets $0.75 \cdot V_{DD}/I_{DSAT}$ instead of $\sim 0.72 \cdot V_{DD}/I_{DSAT}$.
 - Why did we do it this way vs. the book's method?

The Book's Method

The Transistor as a Switch



The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} ($W/L=1$) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L=L_{min}$). For larger devices, divide R_{eq} by W/L .

V_{DD} (V)	1	1.5	2	2.5
NMOS ($\text{k}\Omega$)	35	19	15	13
PMOS ($\text{k}\Omega$)	115	55	38	31