

*EE141-Spring 2008
Digital Integrated
Circuits*

Lecture 8
Inverter Delay and Power

EECS141 Lecture #8 1

Announcements

- Homework #3 due today
- Homework #4 posted today, due next Fr
- Midterm1 Friday February 29 6:00-7:30pm
 - Open book
 - Will cover Lecture 1-8 (not including power)

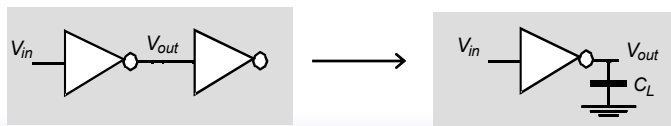
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Class Material

- Last lecture
 - MOS capacitances
- Today's lecture
 - Inverter delay
 - Power dissipation
- Reading (3.3.2, 5.4, 5.5)

Simplified Model

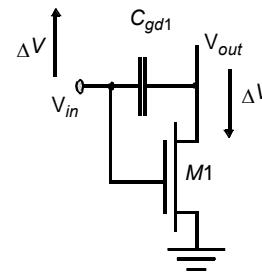
- Capacitance models important for analysis and intuition
 - But often need something simpler to work with
- Simpler model:
 - Lump together as effective linear capacitance to (ac) ground
 - In most processes: $C_g = C_d = 1.5 - 2\text{fF}\cdot W(\mu\text{m})$



Review – MOS Capacitances

The Miller Effect

- As V_{in} increases, V_{out} drops
 - Once get into the transition region, gain from V_{in} to $V_{out} > 1$
- So, C_{gd} experiences voltage swing larger than V_{in}
 - Which means you need to provide more charge
 - Makes C_{gd} look larger than it really is
- Known as the “Miller Effect” in the analog world



Review – MOS Capacitances

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Review – MOS Capacitances

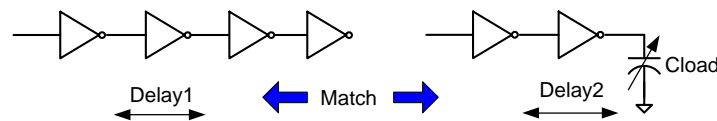
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Model Calibration - Capacitance

- Can calculate C_g , C_d based on tech. parameters
 - But these models are simplified too
- Another approach:
 - Tune (e.g., in spice) the linear capacitance until it makes the simplified circuit match the real circuit
 - Matching could be for delay, power, etc.

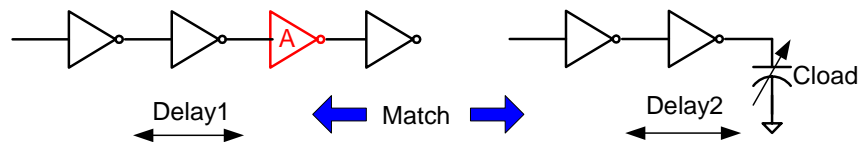


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Model Calibration for Delay



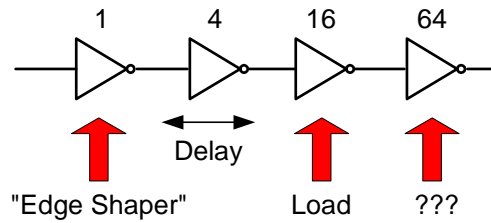
- For gate capacitance:
 - Make inverter fanout 4 (will see why in 2 lectures)
 - Adjust C_{load} until $Delay1 = Delay2$
- For diffusion capacitance
 - Replace inverter “A” with a diffusion capacitance load

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Delay Calibration

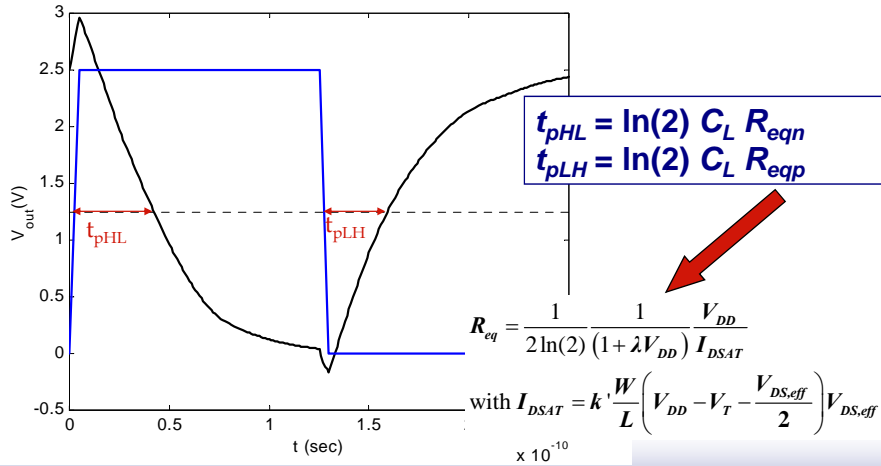


- Why did we need that last inverter stage?

Propagation Delay



Transient Response

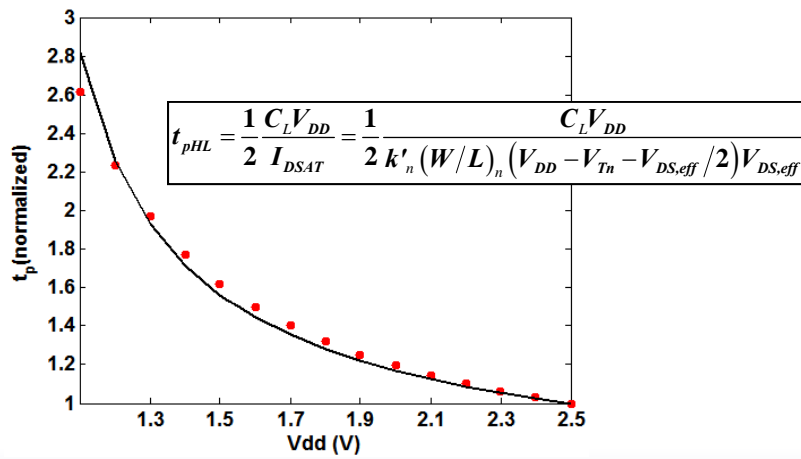


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Delay as a function of V_{DD}

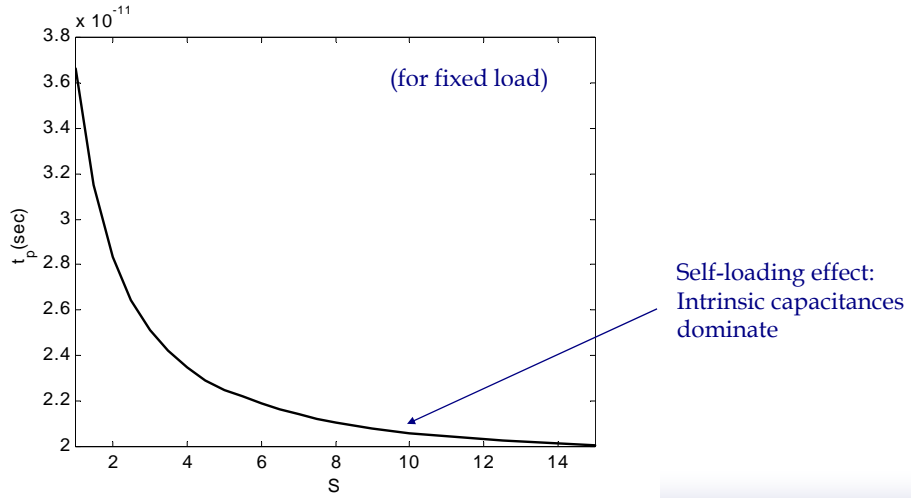


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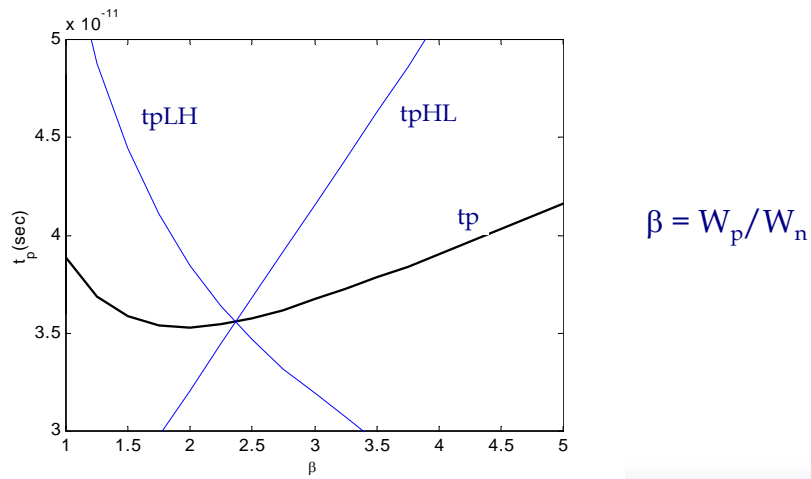
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Device Sizing



NMOS/PMOS ratio

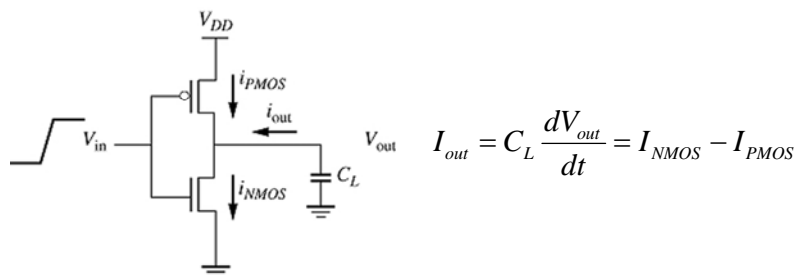


Step Inputs?

- Derived RC model assuming input was a step
 - But input is not a step
 - Transistor turns on gradually

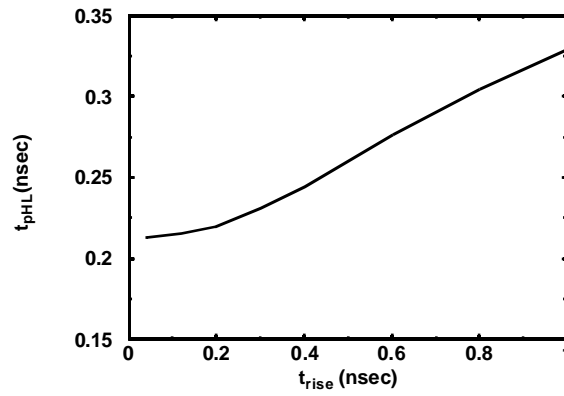
- Let's look at gate switching more carefully
 - Use our models to understand the effect of input slope

Input Slope Dependence



- One way to analyze slope effect
 - Plug non-linear IV into diff. equation and solve...
- Simpler, approximate solution:
 - Use an approximate model (linear, piece-wise linear)

Impact of Rise Time on Delay



$$t_p = t_{step(i)} + \eta t_{step(i-1)} \quad (n \approx 1/3)$$

CMOS Inverter Power Dissipation



Where Does Power Go in CMOS?

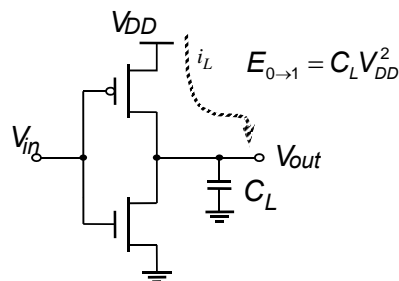
- Switching power
 - Charging/discharging capacitors
- Leakage power
 - Transistors are imperfect switches
- Short-circuit power
 - Both pull-up and pull-down on during transition
- Static currents
 - Biasing currents, in e.g. analog, memory

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Dynamic Power Consumption



$$E_{0 \rightarrow 1} = \int_0^T P_{DD}(t) dt = V_{DD} \int_0^T i_{DD}(t) dt = V_{DD} \int_0^{V_{DD}} C_L dv_{out} = C_L V_{DD}^2$$

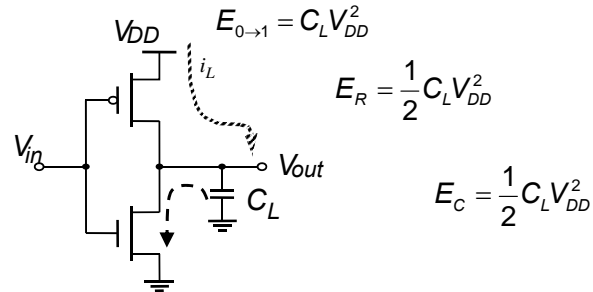
$$E_C = \int_0^T P_C(t) dt = \int_0^T v_{out} i_L(t) dt = \int_0^{V_{DD}} C_L v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

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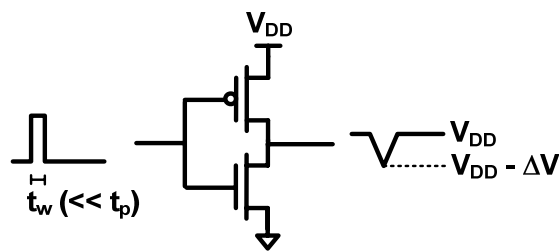
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Dynamic Power Consumption



- One half of the energy from the supply is consumed in the pull-up network, one half is stored on C_L
- Energy from C_L is dumped during the $1 \rightarrow 0$ transition

Circuits with Reduced Swing



$$E_{0 \rightarrow 1} = (C_L \Delta V) V_{DD}$$

Dynamic Power Consumption

Power = Energy/transition • Transition rate

$$= C_L V_{DD}^2 \cdot f_{0 \rightarrow 1}$$

$$= C_L V_{DD}^2 \cdot f \cdot P_{0 \rightarrow 1}$$

$$= C_{switched} V_{DD}^2 \cdot f$$

- Power dissipation is data dependent – depends on the switching probability
- Switched capacitance $C_{switched} = C_L \cdot P_{0 \rightarrow 1}$

Transition Activity and Power

- Energy consumed in N cycles, E_N :

$$E_N = C_L \cdot V_{DD}^2 \cdot n_{0 \rightarrow 1}$$

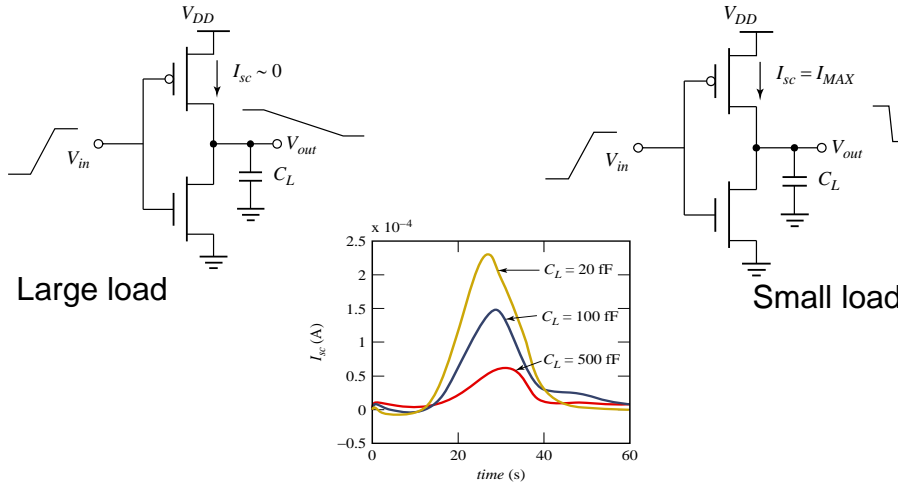
$n_{0 \rightarrow 1}$ – number of 0→1 transitions in N cycles

$$P_{avg} = \lim_{N \rightarrow \infty} \frac{E_N}{N} \cdot f = \left(\lim_{N \rightarrow \infty} \frac{n_{0 \rightarrow 1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0 \rightarrow 1} = \lim_{N \rightarrow \infty} \frac{n_{0 \rightarrow 1}}{N}$$

$$P_{avg} = \alpha_{0 \rightarrow 1} \cdot C_L \cdot V_{DD}^2 \cdot f$$

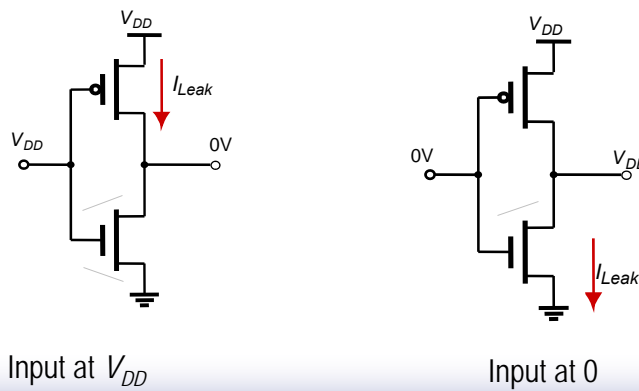
Short Circuit Current



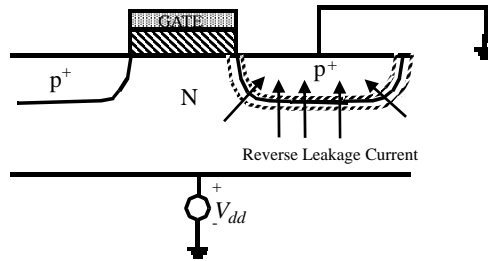
□ Short circuit current usually well controlled

Transistor Leakage

□ Transistors that are supposed to be off - leak



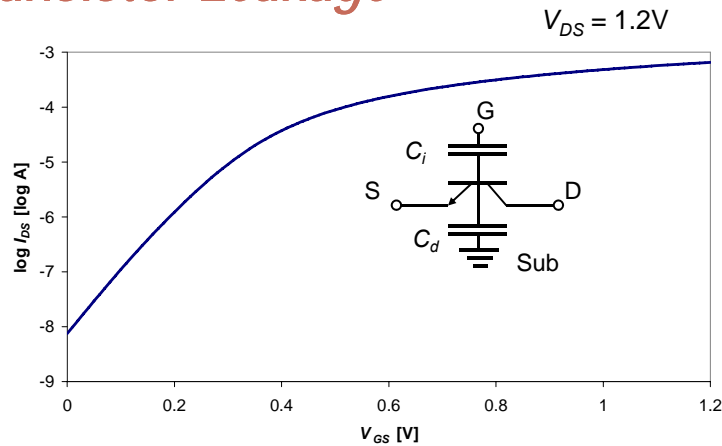
Diode Leakage



$$I_{DL} = J_S \times A$$

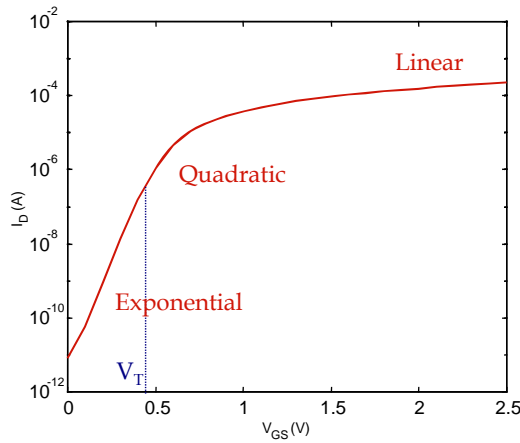
$J_S = 10\text{-}100 \text{ pA}/\mu\text{m}^2$ at 25 deg C for 0.25 μm CMOS
 J_S doubles for every 9 deg C!
 Much smaller than transistor leakage in deep submicron

Transistor Leakage



Drain leakage current is exponential with $V_{GS} - V_T$

Sub-Threshold Conduction



Inverse Subthreshold Slope:

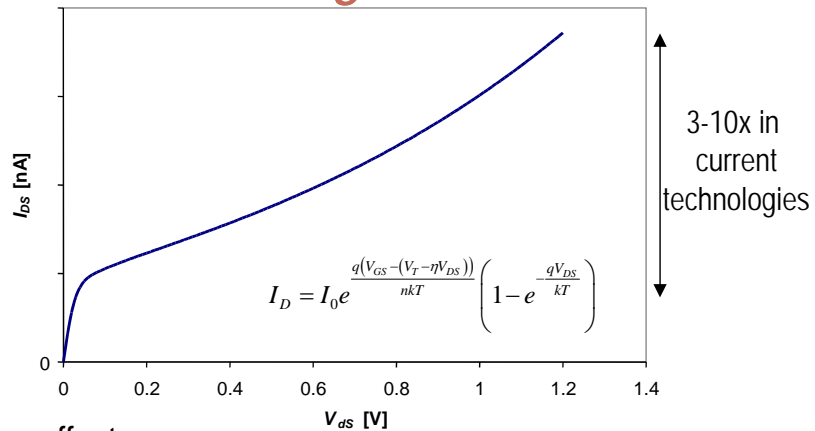
$$I_D \sim I_0 e^{\frac{q(V_{GS}-V_T)}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

S^{-1} is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S^{-1} = n \left(\frac{kT}{q} \right) \ln(10)$$

Typical values for S^{-1} :
60 .. 100 mV/decade

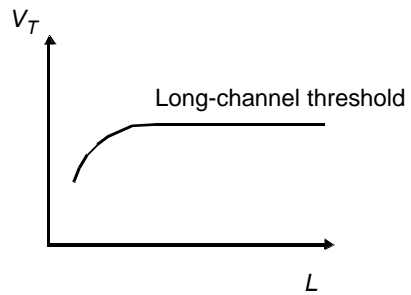
Transistor Leakage



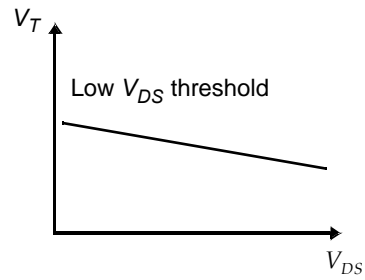
Two effects:

- diffusion current (like a bipolar transistor)
- exponential increase with V_{DS} (η : DIBL)

Threshold Variations



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (DIBL) (for short L)

Next Lecture

- Buffer sizing