

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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EECS 141

Spring 2008

FIR Filter Project – Part 2

Due We, April 23, 5pm @ 240 Cory

High-Level Optimization

In the first phase of the project, we analyzed a straightforward implementation of the FIR filter. Now it is time for the real design work. We will apply everything we have learned in class so far to optimize the design for a specific goal. You get to choose one of the three following goals:

- 1 Minimize delay **without any power concerns**.
- 2 Assuming that you can extend the delay by approx 15% over what you obtained in Phase 1, minimize power. This means that the **worst-case delay should be no more than 1200 ps**.
- 2 Assume that you can increase the power by approx 15% over your first implementation, minimize the delay. This means that the **average power should be no more than 75 μ W**.

You are free to change the topology of the filter, choose any logic design style you like, and/or change the supply voltage. **The input-output response of the filter obviously should remain unchanged.**

In this phase, we will concentrate on high-level optimization. No layout is necessary. Use any tool that can help you to optimize (such as, for instance, MATLAB and SPECTRE). The outcome should be a new netlist, and simulation results that prove your results are for real.

PROJECT DESCRIPTION

Overall logistics:

- 3 You should stick to the partner you have chosen in Phase 1. You should let Prof. Rabaey know if this is no longer possible.
- 4 On Friday April 11, we will rotate a sign-up sheet in class where you will choose between one of the three optimization options mentioned above. In each category, we will allow only a fixed number of entries.
- 5 Project phase 2 report is due on We April 23.

Constraints:

- 6 The maximum supply voltage however is set to 1.2V.
- 7 Also, you have to keep the register cells as is (only the adder cells can be changed).

- 8 The outputs of the filter are loaded with a single register.
- 9 For the computation of the power consumption, use the same waveform as we used in phase 1 (initial value of all the registers should be set to zero).

Report

Please use the report template provided at the website. Be sure to justify important design decisions and emphasize all the vital information. Organization, conciseness, and completeness are of paramount importance. Good reports are short and to the point. Make sure to include and annotate important plots to illustrate your effort. Do not repeat the information we already know. Make sure to fill out the cover-page and use the correct units.

Grading

The quality of the report is a major part of the grade.

For phase 2, the grade will emphasize originality and creativity, accuracy, and the quality of the report.

Have fun, and good luck!