

**UNIVERSITY OF CALIFORNIA**  
**College of Engineering**  
**Department of Electrical Engineering**  
**and Computer Sciences**

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*EECS 141*  
*Spring 2008*

**FIR Filter Project – Part 3**

*Due We, May 7, Afternoon*

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## **Realizing your perfect filter**

Now that you have defined what the perfect realization of the filter should be (given the constraints you selected), it is now time to check if this pans out. In this phase of the project, you will go to a full detailed design. This includes complete transistor schematics, verification of timing and power claims, and layout.

Although you may realize that you still can improve on the design choices you made in phase 2, we strongly suggest that you do NOT go for any major design changes at this time. Focus on verification, realization and meeting the design goals. Area is an issue at this time of the project. The quality of the layout will be a factor. (Remember, the registers are fixed, focus on the adders).

You will present your results to the assembled panel of experts (that is, the TAs and Prof. Rabaey) on We May 7 at a poster session. A sign-up sheet will be circulated in class on We April 30. (if you cannot attend, please check with Prof. Rabaey on available slots).

Please use the report template provided at the website. Be sure to justify important design decisions and emphasize all the vital information. Organization, conciseness, and completeness are of paramount importance. Good reports are short and to the point. Make sure to include and annotate important plots to illustrate your effort. Do not repeat the information we already know. Make sure to fill out the cover-page and use the correct units.

## **Poster**

This time around, you will have the opportunity to present your brilliant design orally to the funding (that is, grading) agents. Be aware that the allotted time for your poster presentation is strictly limited to 10'. In that time you have to convince us not only that you have chosen the right strategy, but also that your design is correct. Use your time (and poster board area) wisely! DO NOT REPEAT WHAT WE ALREADY KNOW (e.g. that you have to design a filter ...). Focus on the essential elements. Given 9-12 slides, make sure to include the following:

- Basic ideas behind your design strategy (from phase 2)
- Overall schematic and topology of your solution, indicating the critical path
- Other important schematics (e.g. your key adder cell)

- Demonstration of functionality of your design
- Verification of the timing results
- Analysis and verification of the power
- Layout of the critical cell
- Overall layout of the filter.

Be aware that of the 10' presentation, at least 3' will be dedicated to Q&A. Hence be concise.

## **Poster Creation Instructions**

- Download the file “ee141\_yourname.ppt” from the website, and rename the file with you and your partner’s names.
- Create your slides (9-12 will fit on the poster board) in PowerPoint using the provided template.
- As indicated in the template, the first slide should include you and your partner’s names.
- For the poster session, you should print your slides on 8.5” x 11” sheets of paper and bring them to BWRC on Thurs. Nov. 29<sup>th</sup> in the afternoon before 3pm. Poster boards will be available for you there for you to glue/paste your printed slides onto.
- Don’t forget to email your final slides to [ee141-project@bwrc.eecs.berkeley.edu](mailto:ee141-project@bwrc.eecs.berkeley.edu). This is **essential**, as the submitted slides are considered the report for this phase.

**Be inspired – and accurate!**