

University of California  
College of Engineering  
Department of Electrical Engineering  
and Computer Sciences

B. Nikolic

Wednesday, May 16, 2001.

5:00-8:00pm

## EE241—SPRING 2001: FINAL EXAM

|             |      |       |
|-------------|------|-------|
| <b>NAME</b> | Last | First |
|-------------|------|-------|

|                       |  |
|-----------------------|--|
| <b>GRAD/UNDERGRAD</b> |  |
|-----------------------|--|

**Problem 1:**

**Problem 2:**

**Problem 3:**

**Problem 4:**

**Problem 5:**

**Problem 6:**

**Problem 7:**

**Total:**

**PROBLEM 1. Scaling. (10pts)**

Please show all the work.

a) In an ideal scaling model, where all dimensions and voltages scale with a factor of  $S$ :

i) (2pts) How does the  $I_{DSAT}/W$  scale?

ii) (2pts) How does the delay of a FO4 inverter scale?

iii) (2pts) How does power scale?

b) (4pts) Over the past 10 years, clock freq for processors has been doubling with each  $S = 0.7$  shrink of technology, by reducing the number of gates in a clock cycle. For this frequency scaling, how would you expect power to scale? Please explain your reason.



c) (8pts) What is the output capacitance value (path electrical effort) for which one design becomes faster than the other? Can you provide an intuitive explanation for this? When would you decide to build logic into the static gates?

**PROBLEM 3. Logic circuits. (22pts)**

a) What process corner (fast (F), typical (T) and slow (S)), temperature, and supply voltage (high (H), typical(T), low(L)) would you use to test the following circuits, or explain why none would be appropriate? Assume the circuit must meet specifications over all process corners. Please briefly explain your reason.

i) (4pts) To measure the delay of a circuit to test the setup time into a flip-flop.

ii) (4pts) To measure the delay of a circuit to test the hold time into a flip-flop

iii) (4pts) Effects of power supply noise on a dynamic circuit.

iv) (4pts) Find the worst case leakage current from a logic gate.

b) (6pts) Show a dual rail dynamic gate that produces the input majority function (generates carry for a full adder). Does this gate have a charge-sharing problem? If it does, show how it can be fixed. Design the gate to keep the stack height small. What is the logical effort of each input?

**PROBLEM 4. Flip-Flops (22pts)**

A pulse-triggered latch is shown in Figure 4a.

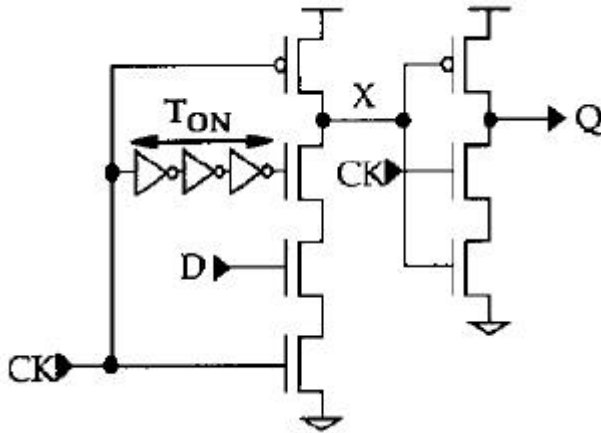


Figure 4a.

a) (2pts) Briefly explain how this circuit works.

b) (2pts) What is the advantage of using this circuit over a conventional master-slave latch pair?

c) (4pts) If  $T_{ON} = 100\text{ps}$  is the propagation delay of three inverters as shown in Figure, and clock-to-output delay  $T_{CLK-Q} = 150\text{ps}$  (with data signal settling long before clock rises), what are the approximate values for the setup and hold times for this circuit?

d) (6pts) Note that this circuit is simpler than pulse-triggered latches shown in the class. Are there any problems that may arise from using this pulsed latch? Please briefly describe three most important ones.

e) (8pts) Figure 4b shows a design of a rising edge flip-flop, consisting of a pulse generator in the first stage and an SR latch in the second stage. Design an equivalent falling-edge flip-flop with similar setup time. (Just placing an inverter on the clock signal will not be accepted as a correct solution, because it will change the setup time). Please explain what you did and label the schematic.

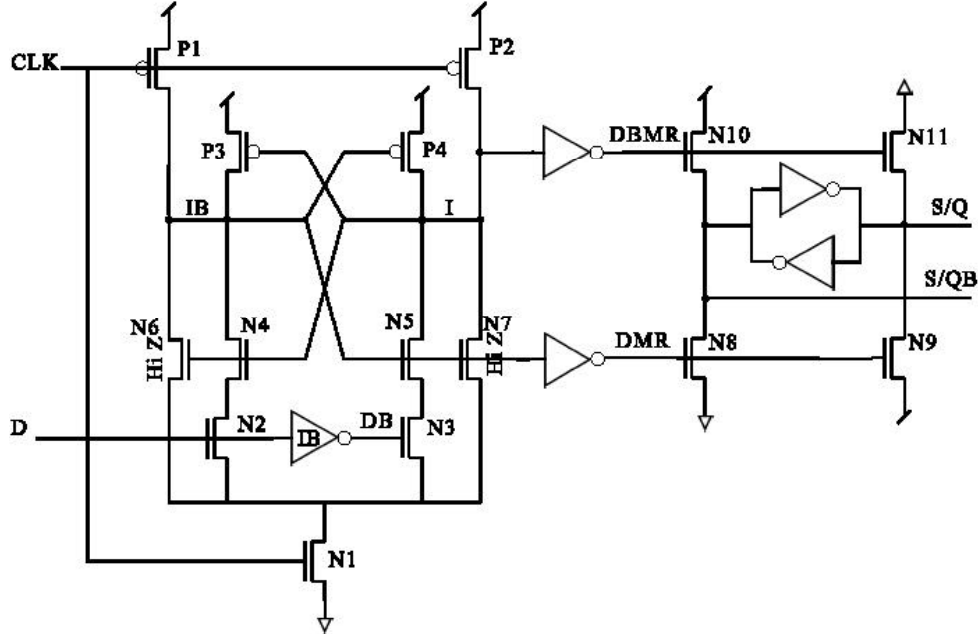


Figure 4b.

**PROBLEM 5. Adders and Multipliers. (10pts)**

a) (4pts) Give two reasons why you might not want to use a domino carry-save adder in a multiplier tree.

b) (6pts) In a precharged Manchester carry chain circuit, find the probability that the carry signal is propagated from the 15<sup>th</sup> to the 16<sup>th</sup> bit of a 32-bit adder, assuming random inputs.

**PROBLEM 6. Timing (18pts)**

An example pipeline with a loop is shown in Figure 6a. L1 latches are transparent when C1 is high, L2 latches are transparent when C2 is high.

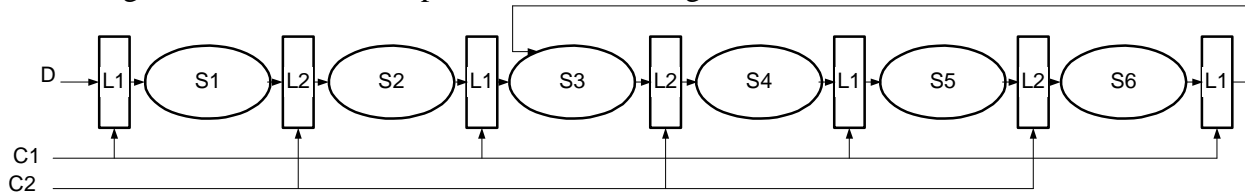


Figure 6a.

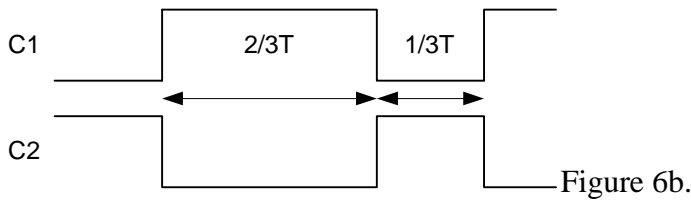


Figure 6b.

The pipeline is clocked by an asymmetric two-phase clocking system as shown in Figure 6b. The clock edges are ideal and both edges of the clocks have a skew of 100ps. Input datum D is available 200ps before the falling edge of the clock C1. Assume that the latches have zero propagation delays and zero setup and hold times. Each of the pipeline stages, S1, S2, S3, S4, S5, and S6 is designed using static logic. Propagation delays of each of the combinational logic stages are  $t_{S1} = 1\text{ns}$ ,  $t_{S2} = 1\text{ns}$ ,  $t_{S3} = 2\text{ns}$ ,  $t_{S4} = 1.5\text{ns}$ ,  $t_{S5} = 3\text{ns}$ ,  $t_{S6} = 1.5\text{ns}$ .

a) (12pts) What is the minimum cycle time of this system? Please show all delay constraints.

b) (6pts) Does any slack passing/time borrowing happen between the pipeline stages?  
Explain and compute the values of slacks passed.

**PROBLEM 7. Interconnect (12pts)**

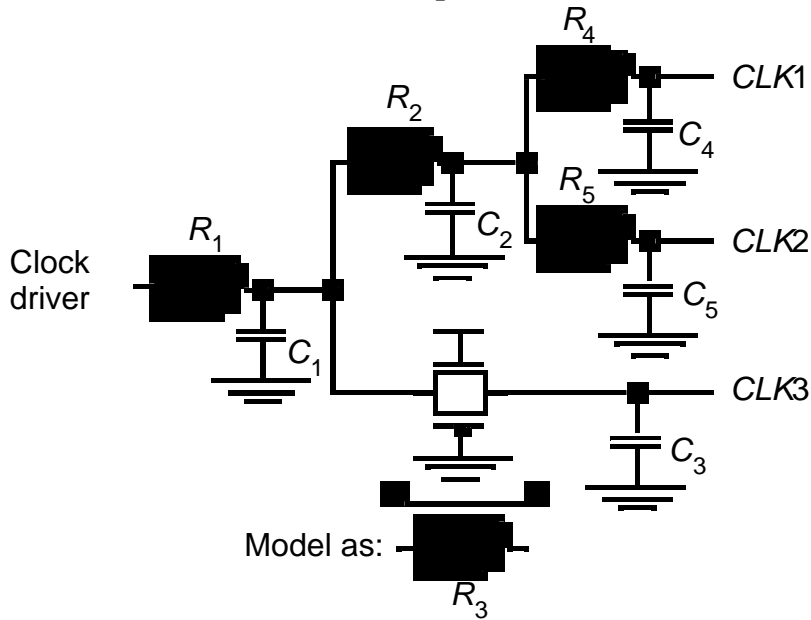


Figure 7.

You are designing a clock distribution network in which it is critical to minimize skew between local clocks (CLK1, CLK2, and CLK3). You have extracted the RC network of Figure 7, which models the routing parasitics of your clock line. Initially, you notice that the path to CLK3 is shorter than to CLK1 or CLK2. In order to compensate for this imbalance, you insert a transmission gate in the path of CLK3 to eliminate the skew. Write expressions for the time-constants associated with nodes CLK1, CLK2 and CLK3. Assume the transmission gate can be modeled as a resistance  $R_3$ .

- a) (10 pts) If  $R_1 = R_2 = R_4 = R_5 = R$  and  $C_1 = C_2 = C_3 = C_4 = C_5 = C$ , what value of  $R_3$  is required to balance the delays to CLK1, CLK2, and CLK3?

b) (2pts) Determine the value of the propagation delay for  $R = 750\Omega$  and  $C = 200\text{fF}$ .