

HOMEWORK 2.**Due: Tuesday, March 11 by 5pm in 558 Cory****This is an individual assignment!****1. Design of complementary networks.**

Design a CVSL gate with minimum number of transistors, implementing the logic function $F = A \oplus B \oplus (C + D)$.

2. Charge Sharing

a) Simulate the charge sharing in a dynamic CMOS gate from Figure 1.a, using Hspice and $0.18\mu\text{m}$ CMOS models. Assume that all the transistors have $1\mu\text{m}$ width and minimum length and that the output is loaded with an inverter ($W(\text{PMOS}) = 2\mu\text{m}$; $W(\text{NMOS}) = 1\mu\text{m}$). What is the voltage drop observed at the output node?

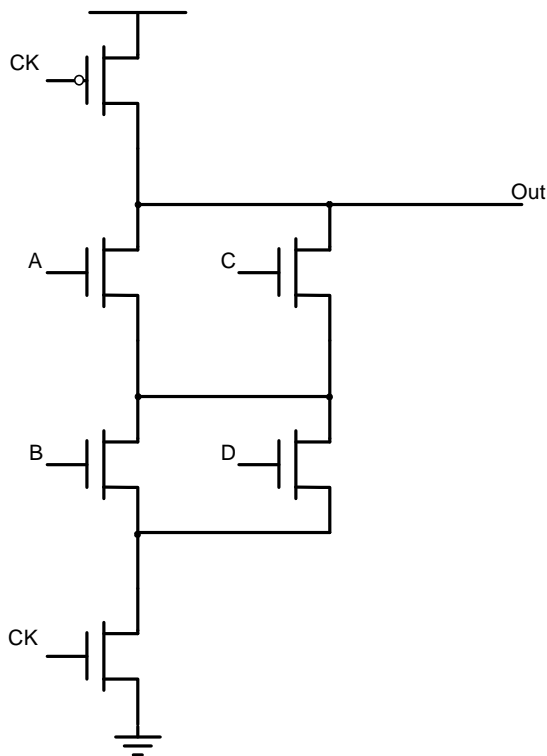


Figure 1.a

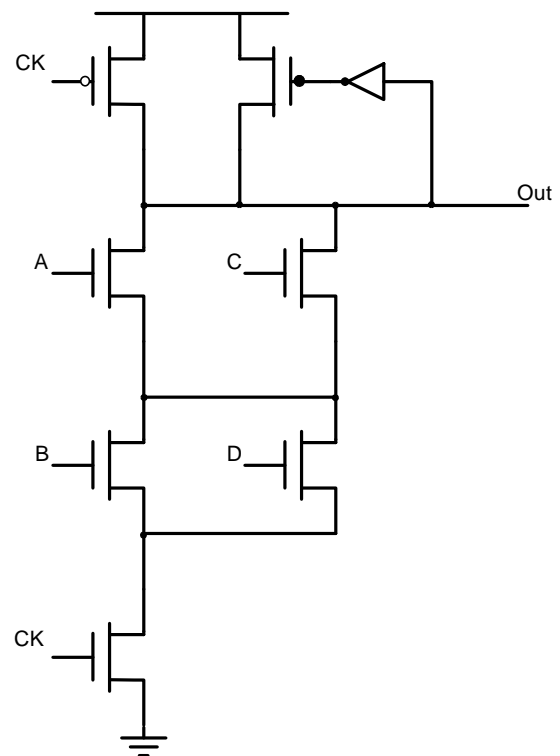


Figure 1.b.

b) Determine the impact on delay of the circuit from Figure 1.a. of:

- adding a static bleeder (minimum L, try $W = 0.25\mu\text{m}$ and $0.5\mu\text{m}$) to the output node.
- precharging the stack node.

- pre-discharging the stack node using a small clocked transistor (stack node pre-discharge). In this case you have to guarantee the reliable operation of the circuit, assuming the external noise can couple a total of 100mV on the dynamic output (inverter input).
- c) Show by simulation the sizing tradeoff of the keeper transistor from Figure 1.b (sizing of the dynamic gate is unchanged from Figure 1.a). Comment the observed results.

3. Decoder design

We will design of a decoder for a 512-word SRAM array, with each word being 256 bits wide, and each bit capacitance presenting one-half of unit inverter load. Address lines $A_8 - A_0$ are available as both true and complementary and may drive up to 4 unit inverter loads. Assume that each of 512 words is independently decoded from 9 input address bits. Use standard, complementary CMOS with symmetrical sizing ($W_p/W_n = 2:1$).

- a) We will design it as a two-level decoder, where the first 4 bits will be pre-decoded. Show a schematic of the decoder for one wordline. Ignore all the wire loads, and size the decoder for optimal speed. Indicate your assumptions, and final transistor sizes.
- b) Realistically the two-level decoder has a large wire load on the predecoded lines, due to the memory array layout. If you assume that memory cells are $3\mu\text{m}$ tall and $4\mu\text{m}$ wide, and that the wire capacitance is $0.2\text{fF}/\mu\text{m}$, calculate the total wire capacitance of each of the predecoded wires. How does it compare to the decoder output capacitance? Assume the predecoded wires are routed vertically and the wordlines are routed horizontally.
- c) Re-formulate the decoder sizing problem, including these wires as a fixed side load after the predecoder stage. Solve it to find new optimum transistor sizes.
- d) After you finished the part c) and estimated the layout area of the design, you found out that the design is too large to fit into its assigned space. You need to decrease the total transistor width in this design by 10%. What would be the minimum achievable delay under this area constraint?